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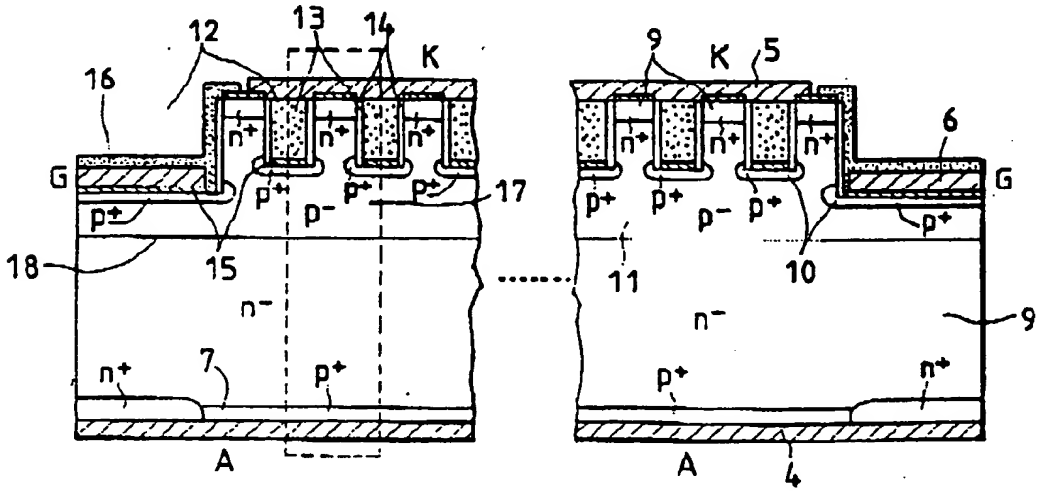
(54) Semiconductor switching device and power converter

(57) There is provided a semiconductor substrate which includes a pair of main surfaces, a first semiconductor layer (7) of a first conductivity type adjacent to one of the main surface, a second semiconductor layer (8) of a second conducting type of which impurity concentration is lower than that of the first semiconductor layer and which is adjacent to the first semiconductivity, a third semiconductor layer (11) of the first conductivity type adjacent to the second semiconductor, and a fourth semiconductor (9) of the second conductivity type of which impurity concentration is higher than that of the third semiconductor and which is adjacent to the other of the main surfaces and the third semiconductor. The device further includes one main electrode (4) in ohmic-contact with the first semiconductor layer on one of the main surfaces of said semiconductor substrate, the other main electrode (5) in ohmic-contact with the first semiconductor layer on the other of the main surfaces of said semiconductor substrate, and a control electrode (6) connected electrically to the third semiconductor layer. The total amount of impurities of said third semiconductor layer is less than $10^{14}cm^{-2}$.

FIG. 1C



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Description

The present invention relates to a semiconductor device particularly suitable to the use in high frequencies and in a large power equipment.

In the fields of a traffic, an industry and an electric power, it is required to develop a high performance gate-turn-off swiching device capable of operating in several kilo-volts and several kilo-amperes. While there is mainly known a GTO thyristor (Gate Turn Off, hereinafter referred merely to as a GTO) as the thyristor of such a type, an SI (Static Induction) thyristor will be able to use in frequencies higher than the operating frequency of the GTO. This is disclosed, for example, in the papers, the 6th SI device symposium (Jan. 1993), SID-92-(1)-1, pages 1 to 6. When the device is operated in the high frequencies, the power loss generated in the device when switched, that is, the switching loss increases in proportion to the frequency. Because the problem that the temperature of the device may increase due to the switching loss is very hard to solve, it is required to decrease a turn-off loss, that is, the loss made when a current is turned off, which occupies a large part of the switching loss. In order to decrease the turn-off loss, thus cut off a period of the turn-off, it is effective to cut off the life time of carriers by emitting an electron beam or a γ ray to the device so as to speed up the disappearance of the carriers. However, if the life time is cut off, the amount of the carriers in a stationary on-state is decreased. Therefore, the potential drop of the device occurs, thus the on-voltage increases. As a result, the stationary state loss when in the on-state or the on-state loss increases. As seen from the matter described above, there is a trade-off relationship between the turn-off loss and the on-state loss. Accordingly, in high frequencies, it is desirable to use such a device that can inhibit the increasement of the on-voltage and can decrease the turn-off loss.

From the above point of view, the GTO thyristor and the SI thyristor will be compared with each other.

The GTO has a p base layer with high impurity concentration. If the life time of carriers is cut off to a certain extent, that of the carriers in the p base layer also becomes short. Therefore, the number of electrons extremely decreases, which is injected from a cathode and can arrive at an n base layer through the p base layer. Accordingly, even if the turn-off loss can be decreased to a certain extent, an undesirable effect such as the sudden increasement of the on-voltage occurs strongly with it. While, because the SI thyristor has not the p base layer with the high impurity concentration, it is possible to decrease the turn-off loss by cutting off the life time, with suppressing the increasement of the on-voltage. Because, in the SI thyristor, the injection efficiency of an electron is very high, the loss becomes lower. In addition, it is possible to decrease further the loss by increasing the carrier concentration on the side of the cathode in an n- layer more than that on the side of the anode.

However, there are some problems on the blocking voltage of a thyristor with a high blocking voltage, of which the rated voltage is more than 4.5 kV. Because the SI thyristor has not the layer corresponding to the p base layer of the GTO, an anode voltage is blocked by forming an negative potential barrier in a channel due to a gate potential. Therefore, if a high inverese bias voltage is not applied to the gate, the high anode voltage can be blocked. In addition, because the SI thyristor has not the layer corresponding to the p base layer of the GTO and it is impossible to accept the anode voltage by a horizontal pn junction, it is difficult to make a device with a high blocking voltage. Further, because in the SI thyristor, depletion layers pinch the channel, expanding from the p-type gate layers next to each other through the channel and thus block the anode voltage, the width of the channel may effect greatly on the blocking voltage. In other words, the dispersion of the work of the p-type gate layer may affect greatly on the blocking voltage. If there is such a portion in the device where the blocking voltage is low, the blocking voltage of the whole device may be limited within that of the portion. It is, therefore, difficult to obtain the desired blocking voltage with good yield.

There is shown the conventional method of improving the characteristic of the blocking voltage of the SI thyristor in Japanese Patent Application Laid-Open No.61-100966 (1986), in which means for providing the p- layer with low concentration adjacent to the p-type gate layer. However, if the concentration of the provided p- layer is unexpectedly low or the distribution of the concentration is not considered, the effect of the blocking voltage improvement can not be expected. In this prior art, when the anode voltage is low and the contact of the gate is opened, the corresponding space charge region reach an n+ emitter. Thereby, the thyristor can be switched. Namely, the total amount of the impurities in the p-layer with low concentration is suppressed so as to indicate the normally-on characteristic. If the circuit between the gate terminal and the cathode terminal is unwillingly opened or short-circuited when the anode voltage is blocking by the application of an inverse bias to the gate under the condition of the low concentration p-layer, it becomes impossible to block a high anode voltage, thus the device is apt to mistake in operation.

The present invention is made under the consideration of the above-mentioned problems.

An object of the present invention is to provide a semiconductor device which has both the characteristics of a high blocking voltage and a lower loss.

The summary of the invention will be explained hereinafter, where, the concentration of impurities designates an absolute value of the difference between the concentration of acceptor impurities and that of donor impurities, the substantial conc ntration of impurities. Further, the total amount of impurities designates the amount corresponding to the substantial concentration of impurities.

A semiconductor device of the present invention is provided with a semiconductor substrate which includes

a pair of main surfaces, a first semiconductor layer of a first conductivity type adjacent to one of the main surface, a second semiconductor layer of a second conducting type of which impurity concentration is lower than that of the first semiconductor layer and which is adjacent to the first semiconductivity, a third semiconductor layer of the first conductivity type adjacent to the second semiconductor, and a fourth semiconductor of the second conductivity type of which impurity concentration is higher than that of the third semiconductor and which is adjacent to the other of the main surfaces and the third semiconductor.

The semiconductor device according to the present invention further includes one main electrode in ohmic-contact with the first semiconductor layer on one of the main surfaces of said semiconductor substrate, the other main electrode in ohmic-contact with the first semiconductor layer on-the other of the main surfaces of said semiconductor substrate, and a control electrode connected electrically to the third semiconductor layer.

Further, the total amount of impurities of said third semiconductor layer between said second semiconductor layer and said fourth semiconductor layer is less than $10^{14}cm^{-2}$.

In the semiconductor device according to one of the preferred embodiment of the present invention, the total amount of the impurities of the third semiconductor layer between the second semiconductor layer and the fourth semiconductor layer is in the range of $10^{12}cm^{-2}$ to $10^{14}cm^{-2}$.

According to the present invention, it is possible to improve the blocking voltage, because the applied voltage can be blocked by a junction of the second semiconductor layer of the first conductivity type and the third semiconductor layer of the second conductivity type in an off-state. It is further possible to increase the amount of carriers injected from the fourth semiconductor layer to the second semiconductor layer, because the transport factor of the carriers is improved in the third semiconductor layer by setting the total amount of the impurities of the third semiconductor so as to be less than $10^{14}cm_{-2}$, which is provided between the second semiconductor layer and the fourth semiconductor layer. As a result, it becomes possible to suppress the on-voltage so as to be low due to the cut-off of the lifetime of the carriers, even if the turn-off loss is decreased. Namely, the semiconductor device according to the present invention has both the characteristics of a low on-voltage and a low turn-off loss.

Further, according to the present invention, the total amount of the impurities of the third semiconductor layer between the second semiconductor layer and the fourth semiconductor layer is in the range of $10^{12}cm_{-2}$ to $10^{14}cm_{-2}$. It is possible to block a voltage regardless of the presence or absence of a signal or the polarity of a control electrode, by setting the total amount of the impurities of the third semiconductor layer so as to be equal to or more than $10^{12}cm^{-2}$, and obtain a normally-off characteristic.

Fig.1A is a plan view of the whole device of a recess gate type according to a first embodiment of the present invention.

Fig.1B is a plan view of a segment of the recess gate type device.

Fig.1C is a sectional view of a segment of the recess gate type device.

Fig.2A is a sectional view of a peripheral region of the recess gate type device according to the first embodiment of the present invention.

Fig.2B is a sectional view of a unit element.

Figs.3A to 3F are sectional views of the neighborhood of a cathode of the unit element.

Fig.4A is a graph representing the relationship between the total amount Q of the impurities and the anode blocking voltage and that between the total amount Q and the on-voltage.

Fig.4B is a graph representing the relationship between the total amount Q of the impurities and the anode blocking voltage and that between the total amount Q and the turn-off loss.

Fig.5 is a graph representing the relationship between the total amount Q of impurities and the anode blocking voltage.

Figs.6A and 6B are schematic views illustrating an inner state of the device short-circuited between the gate and the cathode.

Fig.7 is a graph representing the distribution of the impurity concentration in the vertical direction of the device or element and that of the electron concentration at the normally-on of the device.

Fig.8 is a graph representing the relationship between an on-voltage and a turn-off loss.

Figs.9A to 9J each is a schematic view of the step of a manufacturing process of the device.

Figs.10A and 10B are a gragh and a table showing an example of the impurity distribution of a p- layer produced by using the manufacturing process shown in Figs.9A to 9J and conditions thereof, respectively.

Figs.11A is a graph representing the relationship between the total amount Q' of impurities and the anode blocking voltage.

Figs.11B is a graph representing the relationship between the total amount Q" of impurities and the anode blocking voltage.

Figs.11C is a graph representing the relationship between the anode blocking voltage and the dimension l_2 of a p+ layer, and that between the on-voltage and the dimension l2.

Figs.12A to 12C are illustrations of the mechanism of Fig.11A.

Figs.13A to 13C are illustrations of the mechanism of Fig.11B.

Fig.14 is a graph representing the impurity distribution in a modification of the first embodiment.

Figs.15A to 15C are views ach showing a plane pattern of a cathode n+ layer.

Figs.16A and 16B are views showing a modification of the first embodiment.

Figs.17A and 17B are views showing an example in which a silicide layer is inserted between an anode p layer and an aluminium layer of an anode electrode in Fig.16.

Figs.18A to 18C are views showing an element of a buried gate type according to a second embodiment.

Figs.19A to 19C are views showing an element of a buried gate type according to a second embodiment.

Figs.20A and 20B are a gragh and a table showing an example of the impurity distribution of a p- layer and conditions thereof, respectively.

Figs.21A to 21F are views showing other embodiments of the present invention.

Fig.22 is a circuit diagram showing an example of a power converter using the semiconductor device according to the present invention.

Fig.23A is a schematic view showing a conventional recessed gate type SI thyristor.

Fig.23B is a schematic view showing a conventional GTO.

Figs.1 and 2 show the structure of a 4.5 kV device or element according to an embodiment of the present invention. Fig.1A shows a schematic plane pattern, Fig.1B a sub-unit of a semiconductor device or the plane pattern of a segment, and Fig.1C a schematic sectional view of the structure of the segment. Fig.2A shows a schematic sectional view of the structure of the periphery portion of the device, and Fig.2B the minimum unit of the semiconductor device forming a segment or a schematic sectional view of the unit device. In Fig.1A, a hatched part 1 has a segment and a gate wiring region. Like many conventional GTOs, a plurality of segments are arranged radially toward the center of a circle. Numeral 2 designates a gate electrode. The gate wiring in the hatch part 1 is connected to the gate electrode, and pass the gate current through the gate electrode. Numeral 3 is a peripheral region required to obtain the necessary blocking voltage.

Referring now to Figs.1B and 1C, there is shown the structure of the segment. The structure in which a gate is provided on the bottom of a groove 12 like this is generally called as a recessed gate type. Hereinafter, the device of a recessed gate type will be referred to as a first embodiment. Numeral 4 designates an anode electrode (a first main electrode), and 5 a cathode electrode (a second main electrode). A gate wiring 6 connected to the gate electrode 2 is provided in the periphery of the segment. The gate wiring 6 functions as a gate electrode to the segment, and is therefore called also a gate electrode (a control electrode). Numeral 7 designates a p+ layer (a first semiconductor layer) for injecting holes, numeral 8 n- layer (a second semiconductor layer) with the impurity concentration lower than that of p+ layer 7, numeral 9 n+ layer (a fourth semiconductor layer) for injecting lectrons, numeral 10 a p+ layer of the gate (a fifth semiconductor layer), and numeral 11 p- layer (a third semiconductor layer). The p- layer 11 isolates the n- layer 8 from the gate p+ layer 10 and the cathode n+ layer 9. As described in detail later, the total amount of the impurities of the p- layer 11 between the n- layer 8 and the n+ layer 9 should be at least less than $10^{14}cm^{-2}$.

In the present embodiment, the pn junction 18 of the p- layer 11 and n- layer 8 is in a plane form, and an anode short-circuit structure is adopted. In addition, a groove 12 is provided for forming a gate portion and is filled with a resin 13 such as polyimide. Numeral 14 designates a silicon oxide provided for stabilizing the characteristic of the surface of the side wall of the groove. Numeral 15 designates a silicide layer with a low resistance which functions as the gate wiring in the segment, and 16 a resin layer for passivation of the device. $TiSi_2$ (titanium silicide) can be used as a silicide material.

As seen from Figs.1A and 1B, the segment has the structure in which a plurality of smaller unit devices 17 are arranged. Fig.2B shows a section of the unit device. While, Fig.23A is a sectional view showing the unit device of a conventional recessed gate type SI thyristor, and Fig.23B is a sectional view showing the unit device of a conventional GTO. The conventional SI thyristor has not the p- layer 11 and the p layer 30 of a conventional GTO has large total amount of the impurities and the impurity concentration higher than that of the p- layer 11 of the present embodiment.

Fig.3 shows a section in the neighborhood of the cathode 5 of the unit device 17. The definition of the area of the gate p+ layer 10 of the present embodiment will be explained with reference to Fig.3. The gate p+ layer 10 is formed as a gate layer, has the same conductivity type as the p- layer 11, but has the impurity concentration higher than that of the p- layer 11. Namely, the magnitude of the impurity concentration in this region can not be disregarded compared with the p- layer 11. The following definition is made in consideration of the above matter.

Fig.3A is an enlarged view showing the neighborhood of a gate wiring layer 15. In the present embodiment, the maximum impurity concentration of the gate p+ layer 10 of the gate adjacent to the gate wiring layer 15 is basically larger than $1 \times 10^{18}cm^{-3}$. The impurity concentration in region 20 is 1/10 of the maximum impurity concentration. The distance is set to l_1, which measured from the bottom of the groove 12 to the position nearest to the n- layer 8 of the region 20 (in this case, it is in plane). The gate p+ layer 10 is formed within the region where the distance l_2 from the bottom of the groove 12 is smaller than $3 \times l_2$.

Fig.3B shows the definition of channel width W. The region between the gate p+ layers 10 is defined as a part of the channel. The shortest distance between the gate p+ layers 10 is defined as channel width W. In the present embodiment, the channel width is set to a value between several μm and several tens of μm in order to increase the turn-off capability. the grade of concentration of the gate p+ layer 10 is very large. Accordingly, th defined channel width W can be in fact the same as that d fined

as the shortest distance between the gate p+ layers 10 in the prior art SI thyristor in which the channel is the n-region 8.

Numeral 21 of Fig.3C designates the region penetrating through a low concentration layer 11 in a vertical direction. The amount Q converted the total amount of the impurities in this region into the amount per unit area of cross section, is called as the total amount of the impurities in the p- layer 11. It is desired that the value of Q is in the range of smaller than $10^{14}cm^{-2}$, or larger than $10^{12}cm^{-2}$ and smaller than $10^{14}cm^{-2}$, preferably larger than $10^{12}cm^{-2}$ and smaller than $10^{13}cm^{-2}$. This value of Q is constant with regard to the region with the arbitrary area and position penetrating the low concentration layer. For example, this region can be selected as numeral 211 of Fig.3D.

The effect of the total amount Q of the impurities to the characteristics will be explained hereinafter.

Figs.4A is a graph representing the relationship between the total amount Q of the impurities and the anode blocking voltage and that between the total amount Q and the on-voltage. The on-voltage is adjusted substantially to the same value as the turn-off loss. The device which the p- layer is provided and which satisfies $0 < Q \leqq 10^{14}cm^{-2}$ has the anodo blocking voltage much higher than that of the conventional SI thyristor and has the on-voltage much lower than that of the conventional GTO. Further, the device which satisfies $10^{12}cm^{-2} \leqq Q \leqq 10^{14}cm^{-2}$ has especially higher anode blocking voltage. Furthermore, the device which satisfies $10^{12}cm^{-2} \leqq Q \leqq 10^{13}cm^{-2}$ has almost the same low on-voltage as the conventional SI thyristor and has almost the same high blocking voltage as the conventional GTO.

Figs.4B is a graph representing the relationship between the total amount Q of the impurities and the anode blocking voltage and that between the total amount Q and the turn-off loss. Where, the on-voltage is adjusted substantially to the same value as the turn-off loss. The device which the p- layer is provided and which satisfies $0 < Q \leqq 10^{14}cm^{-2}$ has the anode blocking voltage much higher than that of the conventional SI thyristor and has the turn-off loss much lower than that of the conventional GTO. Further, the device which satisfies $10^{12}cm^{-2} \leqq Q \leqq 10^{14}cm^{-2}$ has especially higher anode blocking voltage. Furthermore, the device which satisfies $10^{12}cm^{-2} \leqq Q \leqq 10^{13}cm^{-2}$ has almost the same low turn-off loss as the conventional SI thyristor and has almost the same high blocking voltage as the conventional GTO.

Next, the reason why the characteristic difference occurs due to the total amount Q of the impurities will be explained.

Fig.5 is a graph representing the relationship between the total amount Q of the impurities in the p- layer 11 and the anode blocking voltage. the channel width is used as a parameter. It is assumed that the circuit between the gate and the cathode is opened. The conventional SI thyristor has not the p- layer 11. Therefore, if an inverse bias voltage is not applied to the gate, it is difficult to form the potential barrier in the channel. Therefor, if the circuit between the gate and the cathode is opened, it is possible to block the anode voltage if the channel width is very short, but the device goes in on-state, in other words, it has normally-on characteristics if the channel width is slightly long. As explained above, the blocking voltage of the conventional SI thyristor is extremely affected by the channel width. In the device which the total amount Q of the impurities is larger than $0\ cm^{-2}$ ($Q > 0\ cm^{-2}$), or which the p- layer is provided, the blocking voltage can be improved and the dependence of the blocking voltage to the channel width W is lessen. However, if the total amount Q of the impurities satisfies $Q < 10^{12}cm^{-2}$, the depletion layer easily reach cathode n+ layer 9, that is, the device goes in a punch-through state. Accordingly, the blocking voltage is low. If the channel width is narrow, it is possible to prevent the punch-through. However, if the channel width is wide, it is impossible to prevent that. On the contrary, as the total amount Q of the impurities increase, the distance of the potential barrier is increased. As a result, When the total amount Q becomes to satisfy $Q \geqq 10^{12}cm^{-2}$, the breakdown due to the punch-through diminishes and the blocking voltage is heighten. Therefore, as explained in detail later, the blocking voltage will depend on the avalanche breakdown. In addition, the dependence of the blocking voltage to the channel width W is also lessen, because the pinching effect of the depletion layer between the neighboring gates is not required to prevent the punch-through. The anode blocking voltage is almost the same when the circuit is opened between the gate and the cathode, when short-circuited, or when an arbitrary and applicable inverse voltage is applied between the gate and the cathode. In all cases, the normally-off characteristics is obtained. The blocking voltage characteristic of the device according to this embodiment is almost the same as that of the GTO. In addition, the turn-on by mistake made by dV/dt of the anode voltage or a leakage current is difficult to occur like the GTO.

Now, if the blocking voltage depends upon the avalanche breakdown, there is an advantage in ease of use. According to the device of the present invention, it is possible to block almost the same anode voltage when the gate is inversely biased and also when the terminal of the gate is opened. Generally explaining, the blocking voltage hardly depends upon the bias state of the gate. More strictly speaking, when the inverse bias is applied to the gate, the blocking voltage decreases by the corresponding voltage to the inverse bias of the gate. However, the blocking voltage difference due to the gate bias state is of the order, at most 5 % of the rated blocking voltage. Therefore, in case of the fault of the gate circuit or the disconnection, th turn-on by mistake does not occur. Further, the malfunction by the short-circuit between the gate and the cathode- does not occur.

Figs.6A and 6B shows an inner state of the device short-circuited between the gate and the cathode. Fig.6A

shows the inner state of the device in which the total amount Q is smaller than that of the device according to the present embodiment. The depletion layer expanded from a pn junction 18 easily reach the cathode n+ layer 9, in other words, it goes in the punch-through state. Therefore, the current as shown by the arrow of the solid line flows to the cathode electrode 5. Further, a current flows to the gate electrode 2 through the gate p+ layer. These currents flow in a state in which an amount of carriers is inadequate, that is, in an incompletely latched state in which the applied voltage of the anode is high. Therefor, in this operating condition, the device is easy to be destroyed by the dispatched heat and thus dangerous. Fig.6B shows the internal state of the device according to the present embodiment. Because the depletion layer does not come to punch through the cathode n+ layer, it is possible to block adequately the anode voltage even when the circuit is opened between the gate and the cathode. When the anode voltage is heighten to the breakdown voltage, the avalanche breakdown occurs. As a result, most of the avalanche currents flow to the gate as shown by an arrow of the dotted line. Therefore, even when the gate circuit operates abnormally, the device according to the present invention can block confirmly the anode voltage. Accordingly, the high reliability of the gate circuit and the simplification of the protective circuit can be attained.

The effect of the total amount Q of the impurities on the on-voltage and the turn-off loss will be explained hereinafter.

Fig.7 is a graph showing the distribution of the impurity concentration in the vertical direction of the element and that of the electron concentration at the normally-on of the device. The figures below is a shematic diagram showing the state of the vertical direction of the device, and the above figure shows the electron concentration in each portion of the schematic diagram. The life time of the n- layer 8 of the device is less than 10 μs. In the above figure, (b) and (c) show the characteristics of the device according to the present invention which has the value of Q. The electron concentration of this device is almost the same as that of the conventional SI thyristor of which characteristic is shown at (a). (d) show the characteristic of the device in which the total amount Q of the impurities of the p- layer 11 is larger than that of the present embodiment, that is, $Q > 10^{14}cm^{-2}$. The electron concentration of the p- layer 11 is very low, compared with other example. Because the life time of carriers of the p- layer 11 becomes short as the total amount Q of the impurities of the p- layer 11 becomes large like this, the efficiency is deteriorated, that the electrons injected from the n+ layer 9 is transported to the p- layer 11 and then reach the n- layer 8. Therefor, the electron concentration becomes low like this. In other words, the feature of the conventional SI thyristor, the large injection efficiency of electrons from the n+ layer 9 to the n- layer 8, is deteriorated.

From the carrier distribution of Fig.7, the relationship between the total amount Q of the impurities, the on-voltage and the turn-off loss can be explained. A so-called tail current which generates a large part of the turn-off loss is produced by the carriers in the neighborhook of the anode p+ layer 7 of this n- layer 8. Therefore, to decrease the carriers which exist herein is effective for the decreasement of the turn-off loss.

In all cases of (a) to (d) of Fig.7, the amount of the carriers in the neighborhood of the anode p+ layer is almost the same, and the life time of the carriers of the n- layer 8 is almost the same. The turn-off loss is, therefore, almost the same. Next, the carrier distribution in the neighborhook of the p- layer 11 of the n- layer 8 will be disscussed. In case of (d), the carrier concentration in the neighborhood of the p- layer 11 of the n- layer 8 is smaller. Therefor, the device with the characteristic (d) has a higher on-voltage than other examples. Namely, if the device with the characteristic (d) has the same turn-off loss as other examples, it has a higher on-voltage than other examples. Therefore, if the total amount Q of the impurities is larger than $10^{14}cm^{-2}$ as shown in Fig.4A, the on-voltage becomes high. If the on-voltage is reduced to the same level as other examples by adjusting the life time of the carriers in the n- layer 8 of the device with the characteristic (d), the turn-off loss becomes larger than that of other devices. Therefore, if the total amount Q of the impurities is larger than $10^{14}cm^{-2}$ as shown in Fig.4B, the turn-off loss becomes larger.

Fig.8 is a graph showing the relationship between an on-voltage and a turn-off loss. The relationship is represented by using the life time of the carriers in the n- layer 8 as a parameter, with regard to each of the devices which have the total amount Q of the impurities in the p- layer 11. In case of the present embodiment (see (b) and (c)), the improved trade-off relationship can be obtained, which is almost the same as the conventional SI thyristor. The device according to the present embodiment has a small on-voltage in the range of the wide turn-off loss. The reason why the trade-off is improved will be explained hereinafter.

In Fig.7, the device according to the present embodiment has the carrier distribution in which the carrier concentration in the neighborhood of the p- layer 11 in the n- layer 8 is larger than that in the neighborhood of of the p+ layer 7 in n- layer 8. It is, thereby, possible to reduce both the on-voltage and the turn-off loss. Such the distribution of carrier concentration can be obtained by suppressing the injection amount of holes from the p+ layer 7 in the side of the anode, using the characteristic in which the injection efficiency of electrons from the cathode is high and using an anode-emitter shorting structure. Because the total amount of impurities of a p base in the conventional GTO is far larger than that of the device with the characteristic (d), if the life time of carrier is longer than that of Fig.7 or 10 μs, the carrier distribution becomes similar to that shown at (d) of Fig.7. Therefor, the trade-off relationship between the turn-off loss and the on-voltage is deteriorated more than the device with

the characteristic (d). If the life time is shortened less than 10 μs in the GTO of a 4.5 kV class, the devic can not be latched, thus can not operate normally. According to the present embodiment, it becomes possible to apply the shorter life time of carrier even in a high blocking voltage device as of 4.5 kV class. In the present embodiment, there is provided the silicon oxide film 14 for passivation on the side wall of the groove 12. this film acts to suppress the surface recombination in the side wall of the groove 12 and prevent the deterioration of the injection efficiency of electrons due to the shorter life time of carrier. Further, because the injection of the electrons is also affected by thickness of the p- layer 11, it is desirable that the thickness of the p- layer 11 is less than 50 μm in case of $Q \leqq 10^{13}cm^{-2}$.

As described above, it is possible to obtain the superior device in the loss by considering the total amount Q of impurities in accordance with the present invention. The less the total amount Q is, the less the turn-off loss in the switching losses is. Therefore, the means for decresing the total amount Q is desirable. In order to obtain a function similar to the anode-emitter shorting structure, it may provide an area in which the life time of carriers is lessen by proton radiation or the formation of an n buffer layer. Further, it may set the concentration of the anode p+ layer 7 to less than $10^{18}cm^{-2}$. It may also use both of them.

It should be noted that it is advantage for low loss to set the total amount Q to $10^{12}cm^{-2} \leqq Q \leqq 6 \times 10^{12}cm^{-2}$ and it is desirable for the anode blocking voltage and its reliability to set $6 \times 10^{12}cm^{-2} \leqq Q \leqq 1 \times 10^{13}cm^{-2}$.

Figs.9A to 9J each is a schematic view of the step of a manufacturing process of the device or element. An n type Si substrate is prepared (Fig.9A), the p- layer 11 is formed by using thermal diffusion of p type impurities (Fig.9B), and the p layer 19 in the periphery of the device is formed by thermal diffusion. After then, the p+ layer 7 in the anode side and the n+ layer are formed (Fig.9D), and the n+ layer in the cathode side is formed (Fig.9E). Next, the groove 12 is formed by anisotrophic dry etching (Fig.9F). After forming the silicon oxide film, the anisotrophic dry etching is performed to the silicon oxide film, thus silicon oxide 14 is left in the side wall of the groove 12 (Fig.9G). The gate p+ layer 10 is formed on the bottom of the groove by using the diffusion of the p type impurities, and the silicide layer 15 is formed self-alignedly on the exposed part of the Si (Fig.9H). After foming the resin layer 13 by buring the groove in the segment with resin (Fig.9I), the resin layer 16 is formed for surface protection of the electrode and the device (Fig.9J). The device is completed after the life time control due to the irradiation of electron rays or γ rays and a packaging process. A p layer 19 in the periphery of the device has the impurities higher than the p- layer 11. Therefore, if the layer is formed by the diffusion due to the same thermal processing, the p layer 19 is formed more deeply, the resultant pn junction has a convex portion. It is not desirable for the blocking voltage. It is possible to adjust the diffusion depth of both layers by diffusing in advance only the p- layer 11 and to make the pn junction 18 to be flat. Even if the impurities of which the diffusion is faster than that of the p layer 19 are used as the impurities of the p- layer 11, this purpose is attained. In the examples of Figs.1 and 2, the p- layer 11 has been formed by ion-implanting borons (B) into the surface and diffusing thermally them. The desired p- layer 11 can be formed by adjusting the B dose amount. It may use Al (Alminium) or Ga (Gallium) as the impurities of the p- layer 11. Further, it may form a diffusion source by the deposition, etc. Because even if there is the dispersion in the condition of the diffusion layer, a high perfomance device can be made stably, it is possible to use a variety of methods for forming the p- layer.

Figs.10A and 10B are a gragh and a table showing an example of the impurity distribution of a p- layer produced by using the manufacturing process shown in Figs.9A to 9J and conditions thereof, respectively. the p-layer 11 and the gate p+ layer 10 show the distribution of impurities along the Gauss distribution. Thereby, it is possible to heighten the gate blocking voltage. In a condition C, the gate blocking is 80 volts and in the remainder conditions, they are 100 volts to 180 volts. the impurity total amount Q' and Q" and the dimension l_2 shown at table 1 are also important quantity for the characteristics. The effect of the desirable numeral range of the total amount Q' and Q" and the dimension l_2 will be explained next.

Firstly, the definition of Q' and Q" will be described. The definition of the l_2 has been already explained with respect to Fig.3.

Numeral 22 of Fig.3E designates a horizontal surface of a part of the gate p+ layer 10 nearest to the n- layer 8, and 23 horizontal surface including the above horizontal surface. Numeral 24 designates an area p- layer 11 in a diretion of the n- layer 8 from the horizontal surface 23. The total amount of the impurities in this region converted into the amount per unit area of cross section, is called as the total amount Q' of the impurities in the n- layer side of the p- layer 11.

Numeral 25 of Fig.3F designates a part of the gate p+ layer 10 nearest to the n- layer 8, and 26 a horizontal surface including the above horizontal surface. Numeral 27 designates an area of the p- layer 11 in a diretion of the n+ layer 9 from the horizontal surface 23. The total amount of the impurities in this region converted into the amount per unit area of cross section, is called as the total amount Q" of the impurities in the n+ layer side of the p- layer 11.

The effect of the total amount Q' and Q" on the characteristics will be explained hereinafter.

Figs.11A is a graph showing the relationship between the total amount Q' of impurities and the anode blocking voltage, in which the voltage between the gate and the cathode is 0 volt. if $Q' \geqq 1.2 \times 10\underline{11}cm^{-2}$, the anode blocking voltage is heightened. In addition, the dependenc of the blocking voltage on the width of a chan-

nel is lessened. Where, the deterioration of the blocking voltage which occurs in the $Q' < 1.2 \times 10^{11}cm^{-2}$ is mild compared with that in the $Q < 10^{12}cm^{-2}$. In other words, by setting to $Q' \geqq 1.2 \times 10^{11}cm^{-2}$, such the mild deterioration of the blocking voltage can be prevented, and by adding the condition $Q \geqq 10^{12}cm^{-2}$, it is possible to obtain confirmly a high blocking voltage and to improve the yield of the device with the high blocking voltage. The devices of Figs.11B and 11C also show a similar characteristic.

Figs.11B is a graph showing the relationship between the total amount Q" of impurities and the anode blocking voltage. Where, the voltage between the gate and the cathode is - 100 V when an anode current is in a turn-off state. In order to improve the characteristic of the anode blocking voltage, it is important suitably to set the condition of Q". If $Q'' \geqq 8 \times 10^{11}cm^{-2}$, the anode blocking voltage is heightened. In addition, the dependence of the blocking voltage on the width of a channel is lessened extremely.

Figs.11C is a graph showing the relationship between the anode blocking voltage and the dimension l2 of a p+ layer, and that between the on-voltage and the dimension l_2. If Q, Q' and Q" are set to more than the predetermined value of the present invention and $1\ \mu m < l_2 \leqq 3\ \mu m$, the anode blocking voltage is heightened and the on-voltage is suppressed to be low.

The mechanism which brings the dependence described above will be explained hereinafter.

Figs.12A to 12C are illustrations showing the mechanism of Fig.11A. They show the position where the distribution of the eqipotential line and the electric field is maximum when the anode voltage of the extent of 400 V is applied. Where, the circuit between the gate and the cathode is opened. Fig.12A shows the case in which the total amount Q' of impurities is smaller than the predetermined range of the present embodiment. The electric field is maximum at the curved portion of the bottom of the gate p+ layer 10. Therefore, the avalanche breakdown is liable to occur therein. When the anode voltage is heighten a little beyond this state, the electric field reach the limited value, the avalanche breakdown occurs, and it is difficult to prevent the higher anode voltage. The reason why the electric field is maximum is as follows.

The space charge region invaded from the pn junction 18 or the depletion layer reach the curved portion of the bottom of the gate p+ layer 10, thereby the depletion layer is produced also in the gate p+ layer 10. Because the space charge density of the depletion layer in the gate p+ layer 10 is higher than that of the p- layer 11, the expansion of the depletion layer in the gate p+ layer 10 becomes less than that in the p- layer 11. Therefore, the equipotential line also is curved at the curved portion of the bottom of the p+ layer, and therefor, the electric field of this portion is strengthened. Fig.12B shows the case that the total amount Q' of impurities is within the predetermined range, but it is relatively small. Because the total amount Q' is large compared with the case of Fig.12A, the invasion of the depletion from the pn junction 18 is lessened. Therefore, the imbalance of the distribution of the electric potential at the curved portion of the bottom of the gate p+ layer 10, that is, the curvature of the equipotential line is lessened. In addition, the amount of the space charges in the gate p+ layer is decreased. As compared with the case of Fig.12A, the maximum electric field is lessened and the avalanche breakdown voltage or the blocking voltage is heightened. Fig.12C shows the case that the total amount Q' of impurities is within the predetermined range, but it is relatively large. By the same reason as the case of Fig.12B, the maximum electric field at the curved portion of the bottom of the gate p+ layer 10 is further lessened. The maximum electric field is produced in the pn junction 18. Under such a condition, the improvement of the blocking voltage is further confirmed. Under the condition of Fig.12A, if the width of the channel is enlarged, the invasion of the depletion layer into the p-layer 11 is increased. Therefore, the curvature of the equipotential line is emphasized, namely, the maximum electric field is heightened. In the device according to the present invention of the cases of Figs.12B and 12C, the invasion of the depletion layer is lessened and the depencence of the maximum electric field on the width of the channel is extremely lessened.

Figs.13A to 13C are illustrations showing the mechanism of Fig.11B. These figures show the distribution of the equipotential line and the position where the electric field is maximum when the anode voltage more than 3000 V is applied. Where, the gate-cathode voltage is - 100 V. Fig.13A shows the case of the conventional SI thyristor which has not the p- layer 11. It becomes possible to produce the potential barrier in the channel and prevent the higher voltage by applying the inverse bias voltage between the gate and the cathode even in the conventional SI thyristor. Because there is not the p- layer 11, the anode voltage is prevented by the curved pn junction which comprises the gate p+ layer 10 and the n- layer 8. Therefore, the equipotential line of the gate electric potential, -100 V and -80 V, is curved along the gate p+ layer. Accordingly, the maximum strength of the electric field exists in the p+ layer 10. Fig.13B shows the case that the device has the p- layer 11, but the total amount Q" is smaller than the predetermined value of the present embodiment. Although there is provided the p- layer 11, the equipotential line of the gate electric potential or -100 V are curved along the gate p+ layer 10 just like the case of Fig.13A. Because the total amount Q" of impurities at the side of the n+ layer 9 in the p- layer is smaller, the depletion layer or the electric field which expands from the pn junction comprising the p- layer 11 and the n+ laye 9 by the gate inverse bias voltage, invades largely into the p- layer 11 and reach the gate p+ layer 10. This depletion layer collides with another depletion layer from the pn junction 18. As a result, the equipotential line is curved largely along the gate p+ layer 10. Hereinafter, this phenominum is referred to as a re-

verse pinch effect. If the total amount Q" Fig.13C is within the predetermined value of the present invention, all the equipotential lines cross the unit device. Therefore, as compared with the case of Figs.13A and 13B, the curvature of the equipotential line is smaller, that is, the maximum electric field is lessened. Because the total amount Q" of impurities is large in this case, the depletion layer due to the gate inverse bias does not reach the gate p+ layer 10, thus the reverse pinch effect is not occurred. Therefore, the electric field is moderated, thus the anode blocking voltage is heightened. If the channel width W is increased under the condition of Fig.13B, the invasion of the depletion layer into the p- layer 11 due to the gate inverse bias is increased. As a result, the curvature of the equipotential line becomes large, that is, the maximum electric field is strengthened. In the device according to the present embodiment shown in Fig.13C, the invasion of the depletion layer into the p- layer 11 due to the gate inverse bias is lessened, thus the dependence of the maximum electric field on the channel width is substantially diminished.

The mechanism in which the dependence shown in Fig.11C occurs will be explained hereinafter.

In the present embodiment, the maximum concentration of impurities of the gate is set to higher than $1 \times 10^{18}cm^{-2}$ in order to decrease the gate resistance. It is not desirable to increase the maximum concentration of impurities of the gate p+ layer 10 from the point of view of the anode blocking voltage. Because the difference between the expansion of the gate p+ layer 10 and that of the p- layer 11 is large when the concentration of the gate p+ layer 10 is high, the electric potential line extremely curves and the amount of the space charge in the gate p+ layer 10 increases. By this effect, it is easy to generate a large electric field at the curved portion of the bottom of the gate p+ layer 10. In order to weaken the electric field, it is required to make the depth 12 from the bottom of the groove 12 of the gate p+ layer 10 deep. Thereby, because the expansion in the lateral direction of the impurity diffusion in the gate p+ layer 10, the curvature of radius of the edge portion of the gate p+ layer 10 can be made large. As a result, the electric field is moderated. However, if the depth l_2 is too large, the on-voltage is unwillingly heightened. The reasons are as follows; (1) the distance in the vertical direction of the electric current passage is made longer, and (2) the area ratio of the current passage between the gate p+ layers 10 is lessened. The depth of the gate p+ layer 10, $1\ \mu m \leqq l_2 \leqq 3\ \mu m$, of the present embodiment is smaller than that of the conventional SI thyristor. Therefore, there is an advantage in a point of the low on-voltage of a device.

As described above, the maximum concentration of impurities of the gate p+ layer 10 is increased to higher than $1 \times 10^{18}cm^{-3}$ in the present embodiment. If the concentration of impurities of the gate p+ layer 10 is high, it is possible to decrease the contact resistance between the gate p+ layer 10 and the gate wiring layer 15 and decrease the parasitic resistance of the gate circuit. As a result, it becomes possible to allow confirmly and in a high speed a current to turn off. If the maximum concentration of impurities of the gate p+ layer 10 is heighten to more than $10^{19}cm^{-3}$, it is possible to form the ohmic-contact even by using an aluminium which a metal silicide or silicon is added, as the gate wiring layer 15. Further, it is possible to decrease largely the parasitic resistance of the gate circuit by using only the gate p+ layer 10 as the gate wiring layer 15. In this case different from the case in which the alminium without additives is used, the migration of the gate wiring layer 15 can be suppressed. Therefore, the gate wiring can be fined in this case. The problem that occurs the fault of the blocking voltage also can be solved, in which the fault is made by a spike pulse when the ohmic-electrode is formed. If the alminium without additives is used as the gate wiring layer 15, there is an advantage that can lessen extremely the resistance of the gate wiring layer 15 itself. It is also effective to adopt the structure in which the alminium that the metal silicide layer or silicon is added between the gate p+ layer and the alminium layer without additives.

The numerical definition of the total amount Q', Q" and the depth l_2 has been described hereinbefore. In the present embodiment, the total amount Q of impurities is set to the smaller value compared with the p base layer 30 of a GTO in order to decrease the loss. Therefor, the depletion layer is relatively easy to invade into the p- layer 11. As a result, although the anode voltage is prevented by the plane pn junction 18, the equipotential line is curved and a large electric field is generated, which occurs an avalanche breakdown. Thereby, the blocking voltage is determined. Further, when a high inverse bias voltage is applied to the gate in order to carry out confirmly and in a high speed the turn-off operation, it is liable to occur the avalanche breakdown due to the reverse pinch effect. Such the tendency can not be found in the conventional GTO which also has the plane junction like the present invention. These tendency is lessened by using above numerical limitation of the total amount Q', Q" and the depth l_2 and the blocking voltage is improved.

Some points to be noted in order to obtain a high blocking voltage will be explained hereinafter.

Firstly, it is required to make such the structure that can be obtain a sufficient blocking voltage at the portion corresponding to the gate electrode 2 of Fig.1A, that is, the peripheral region shown in Fig.2A. Referring to Fig.2A, the structure of a sectional surface of the peripheral region of the device will be explained. The side surface of the device is processed by a beveling machining. A p+ layer 101 and a silicide layer 151 are formed on the peripheral portion of the device in the forming process of the p+ layer 10 and the silicide layer 15. Because the concentration of the p- layer 11 is low, a channel is formed on the surface of the p- layer due to the MOS effect when only the p- layer 11 is formed on the peripheral portion. As a result, a leakag current between the anode and the cathode increases, and the anode blocking voltage deteriorates after a long time periods of use.

However, the p+ layer 101 has the function of preventing the formation of such the harmful channel. The formation of the channel is prevented confirmly by providing a p layer 19 which has the impurity concentration higher than the p- layer 11. Because the p layer 19 has the function of lessening the effect of charges outside of the device on the potential distribution inside of the device, it also can solve the problem that the anode blocking voltage deteriorates after a long time periods of use.

It is also required to consider the moderation of an electric field at a position where the junction structure has the irregularity.

From Figs.1C and 2A, it is understood that the depth of the groove provided with the gate electrode 6 is different from that inside of the segment. This is because the etching rate is different according to the depth of the grooves when they are formed by using the anisotropic dry etching method. The difference of the depth of the grooves becomes large when the width of the grooves inside the segment is fined in order to increase the area ratio of the n+ layer 9 for the low on-voltage. The difference of the depth of the grooves brings that of the position in a vertical direction of the p+ layer 11. This means that the effective width of the channel becomes extremely long. Therefore, in the conventional SI thyristor without the p- layer 11, the unit device in the outermost part of the segment limits an anode voltage to a low one. In order to obtain a high blocking voltage by forming a pn junction in a plane which blocks the anode voltage with the p- layer 11, it is necessary to provide the pn junction between the p- layer 11 and the n- layer 8 in the n- layer 8 side from the bottom of the gate p+ layer 10 of the groove with the gate electrode 6, as shown in Figs. 1C and 2A. The effective Q' is important, the quantity converted the total amount of impurities of the region in the n- layer 8 side from the horizontal surface including the bottom of the gate p+ layer 10 of the groove with the gate electrode 6 in the low concentration layer, the p- layer 11, into the amount per unit area of cross section. It is advantageous for the blocking voltage to allow the effective Q' to be as large as possible, under the condition of $Q \leqq 10^{14}cm^{-2}$; preferably $Q' \geqq 1.2 \times 10^{11}cm^{-2}$. The total amount Q" of impurities in the cathode 9 side of the low concentration layer, the p- layer 11, may be desirable to $Q'' \geqq 8 \times 10^{11}cm^{-2}$. As decribed above, it is possible to fine the width of the groove inside the segment into 10 μm. This contributes to the low on-voltage.

If the p- layer 11 is extremely more shallow than the p layer 19 in Fig.2A, the anode blocking voltage is lessen by the effect of the convex shape of the bottom of the p layer 19. It is desirable to select the depth of the p- layer 11 and the p layer 19 so as that both depth is not diffent from each other, or to form the pn junction in a plane by making the p- layer 11 deeper than the p layer 19 as shown in Fig.2A.

Fig.14 is a graph showing the impurity distribution in a modification of the first embodiment. While to form the groove and then to form the gate p+ layer on the bottom thereof is the same as the previous example, the p- layer 11 is formed by using the epitaxial growth in this example. The control of the total amount of impurities is easy, and the high gate bloking voltage is obtained easily by increasing the total amounts Q, Q' and suppressing the maximum impurity concentration.

An example of the plane pattern of the n+ layer 9 in the first embodiment will be explained hereinafter.

Figs.15A to 15C are views each showing a plane pattern of a cathode n+ layer. the portion marked by n+ designates the n+ layer, and other portions designate the groove 12. The segment is constructed by the combination of the n+ layer 9. A plurality of segments is arranged in a radial direction of a disk-like device or element in a way similar to the conventional GTO. l_5 is in the range of several tens of μm to 300 μm, and l_6 is in the range of 1 mm to 4 mm. In Fig.15A, one plane pattern is rectangular, in which it is possible to increase the area ratio of the n+ layer 9 and easily to obtain the high blocking voltage. In Fig.15B, one plane pattern is square. Because the p+ layer 10 is in a higher density state compared with the example of Fig.15A, it is easy to obtain the high blocking voltage and it is possible to realize a device with higher speed operation and a device with large turn-off capability. The making of a photo mask also is comparatively easy. In Fig.15C, one plane pattern is circular. Because the p+ layer 10 has the highest density compared with the examples of Figs.15A and 15B, it is easy to obtain the highest blocking voltage. Because in either cases, the n+ width 13 is set to the range of several μm to several tens of μm and the p+ layer 10 of the bottom of the groove 12 is in a high density state, the extraction efficiency of holes from the gate when the device is turned off is superior. Therefore, it is possible to obtain a device with high speed operation and a device with large turn-off capability. It is desirable to select the width l_4 of the groove to the range of several μm to aeveral tens of μm.

Figs.16A and 16B are views showing a modification of the first embodiment. In this modification, the anode p+ layer 7 (hereinafter, referred to as an anode p layer) is used instead of the anode-emitter shorting structure. The injection of the holes from anode p layer 7 to n- layer 8 is performed by lessening the impurity concentration of the anode p layer to less than $10^{18}cm^{-3}$. As a result, such a carrier distribution is obtained that the carrier concentration in the neighborhood of the p- layer 11 in the n- layer 8 becomes larger than that in the neiborhood of the anode p layer 7 in n- layer 8. If the impurity concentration of the anode p layer 7 is preferably in the range of $10^{16}cm^{-3}$ to $10^{17}cm^{-3}$, The effect of the improvement of the trade-off between the on-voltage and the turn-off loss. Further, the turn-on is.fast compared with the device having the anode-emitter shorting structure. This is because the injection of holes is started from all of the regions of the anode p layer 7 when turned on.

Figs.17A and 17B are views showing an example in which a silicide layer is inserted between an anode p lay-

er and an aluminium layer of an anode electrode in Fig.16. The silicide layer 28 forms a barrier for stopping the diffusion of alminium from the alminium layer 4, and prevent the diffusion of alminium from the anode electrode aluminium layer 4 into the anode p layer 7. It is, therefore, easy to form the anode p layer with lower concentration. The alminium with silicon added may be used as a material of the anode electrode 4, instead of the silicide layer 28.

(EMBODIMENT 2)

Figs.18A to 18C and Figs.19A to 19C are views showing an device of a buried gate type. The device of this type will be called as a second embodiment hereinafter. Also in this embodiment, the gate p layer is the p+ layer with high impurity concentration. Because it has the burried gate p+ layer 10, the definition of the region of the gate p+ layer 10 is different from that in the first embodiment.

In Fig.19C, numeral 29 designates the position where the impurity concentration in the gate p+ layer 10 is maximum. In this case, it is extremely narrow, so that it may be regarded as a point in fact. Numeral 20 designates the region where the impurity concentration is more than 1/10 one of the maximum concentration. l_1 designates the distance between the position 29 and the portion nearest to the n- layer B of the region 20. The the region within the range of the distance $l_2 = 3 \times l_1$ from the center point 29 is defined as the gate p+ layer 10. On the basis of the definition of the gate p+ layer 10, the total amount Q, Q', Q" and the distance l_2 is set to the same values as the first embodiment.

Because the p- layer with low concentration is comprised of an epitaxial growth layer 111 and a diffusion layer 112 formed before the epitaxial growth, the total amounts Q, Q', Q" can be adjusted easily.

Figs.20A and 20B are a gragh and a table showing an example of the impurity distribution of a p- layer and conditions thereof, respectively. The total amount Q' and Q" can be adjusted independly, namely, the Q' can be adjusted by the amount of the impurities of the diffusion layer 112, and the Q" by the amount of the impurities of the epitaxial growth layer 111. Accordingly, compared with the case of Fig.10, it is easy to obtain the high gate blocking voltage and the high anode blocking voltage at the same time. The conventional SI thyristor of the burried gate type has large and harmful effects (the increasement of turn-on time and an on-voltage, etc.) of auto-doping in which the impurities of the p+ layer 10 is diffused outside Si and re-diffused into the channel region. Because it is possible to maintain the high anode blocking voltage and to make the width of a channel long by providing the p- lay r, such the harmful effects of an out-diffusion is lessen, thus it becomes possible to produce a large device with high efficiency.

(OTHER EMBODIMENTS)

Figs.21A to 21F shows other embodiments of the present invention, and is an enlarged view in the neighborhood of the cathode 5 of the unit device. The cathode n+ layer and the gate p+ layer 10 is isolated from the n- layer 8 by the p- layer 11 in these devices. Further, the total amount of impurities in each portion of the p- layer defined in a way similar to that of Fig.3 is set to the value defined in the above embodiment.

Fig.21A shows the structure in which a slightly low concentration layer 113 is provided along the groove 12. The low concentration layer 113 moderates the electric field in the curved portion of the bottom of the gate p+ layer, and sometimes forms a current path. It is not required to make the gate p+ layer 10 thick, because of the moderating function of the electric field. It is provided just for the ohmic-contact with the gate wiring layer 15. As seen from the above, this device is effective in a view point of a lower on-voltage. Futhermore, the low concentration layer 113 acts to avoid the harmful effect due to the channel formed unwillingly on the surface of the side wall of the groove 12.

Fig.21B shows the structure in which a slightly low concentration layer 115 is provided in the neighborhood of the bottom of the groove 12. The low concentration layer 115 acts in a way similar to that of Fig.21B. It is advantageous for making the on-voltage low, because of the narrow low concentration layer.

Fig.21C shows the structure in which the p- layer 11 is diffused. It is possible to obtain a high blocking voltage, by making the thickness of the p- layer 11 thin and by making the concentration comparatively high. Because the p- layer 11 is thin, it is advantageous to make an on-voltage low. An n- layer 81 between the p- layer 11 and the n+ layer 9 is a portion of the n- substrate with low impurity concentration. Therefore, it is advantageous to make an on-voltage low as compared with the device as described later, in which the n- layer 81 is formed by the epitaxial growth. Because most of the depletion layer expand toward the n- layer 8, it is hard to arise the drop of the blocking voltage due to the reverse pinch effect.

Fig.21D shows a burried gate structure, in which the n- layer is provided between the p- layer 11 and the n+ layer 9. This embodiment also can make effectively a blocking voltage high and make an on-voltage low. In addition, because an pn junction can be formed in a plane, the high anode blocking voltage and the high gate blocking voltage can be obtained.

Fig.21E shows a burried gate structure, in which a slightly low concentration layer 115 is provided along the burried gate layer 10. This structure is also effective to make an on-voltage low by the same reason as one of Fig.21B.

Fig.21F shows a planar diffused gate type structure. According to this embodiment, it is easy to produce and it has a good yield. It is advantageous to make an on-voltage low in a device with a thin p- layer (11).

(EMBODIMENT OF THE POWER CONVERTER)

Fig.22 is a circuit diagram showing an example of a power converter for motor driving circuit, using the semiconductor devices (SW_{11}, SW_{12}, SW_{21}, SW_{22}, SW_{31}, SW_{33}) of the present embodiment 1 as switching elements

Fig.23A is a schematic view showing a conventional recessed gate type SI thyristor. Fig.23B is a schematic view showing a conventional GTO. The inverter unit for one phase is constructed by connecting two switching elements (ex. SW_{11} and SW_{12}) in series. a free wheel diode FD is connected in inverse parallel to each of the switching elements. In addition, a so-called anubber circuit S is connected in parallel to each of the switching elements, for protecting the switching element from the rapid rise-up of the voltage. This snubber circuit is constructed by connecting in series a parallel circuit of a diode SD ans a resistor SR to a capacitor SC. The serial connection point of two switching elements in each phase is connected to each of an alternating current terminals (T_3, T_4, T_5). A three-phase induction motor is connected to the AC terminals. The anodes of the switching elements of the upper arm side are connected in common and are connected to a high voltage side of a DC voltage source at a DC terminal T_1. The cathodes of the switching elements of the lower arm side are connected in common and are connected to a low voltage side of a DC voltage source at a DC terminal T_2. The three-phase induction motor is driven by converting a DC to an AC due to switching operation. A gate circuit for control the switching operation is connected between a gate and a cathode of each switching element of the upper and the lower arm sides.

Because the switching elements has the characteristics of a high blocking vlotage and a low loss, it is possible to produce the inverter equipment with a high blocking voltage and a high efficiency. Further, because a high performance device can be produce effectively, it is possible to realize a high performance system at a low cost. It should be noted that any semiconductor devices according to the present invention can be used in a power converter of the present invention and similar effects are obtained in such a modification.

While the invention has been particularly shown and described with reference to the semiconductor device of 4.5 kV class, it will be understood by those skilled in the are that the foregoing and other changes in form and details can be made therein wiiiiithout departing from the spirit and scope of the invention. Further, it will be appreciated that the conductivity type of each semiconductor device can be inversed.

Claims

1. A semicnductor device comprising:

a semiconductor substrate including;

a pair of main surfaces, a first semiconductor layer of a first conductivity type adjacent to one of the main surfaces, a second semiconductor layer of a second conducting type of which impurity concentration is lower than that of the first semiconductor layer and which is adjacent to the first semiconductivity, a third semiconductor layer of the first conductivity type adjacent to the second semiconductor, and a fourth semiconductor of the second conductivity type of which impurity concentration is higher than that of the third semiconductor and which is adjacent to the other of the main surfaces and the third semiconductor,

one main electrode in ohmic-contact with the first semiconductor layer on one of the main surfaces of said semiconductor substrate;

the other main electrode in ohmic-contact with the first semiconductor layer on the other of the main surfaces of said semiconductor substrate; and

a control electrode connected electrically to the third semiconductor layer;

wherein the total amount of impurities of said third semiconductor layer between said second semiconductor layer and said fourth semiconductor layer is less than $10^{14}cm^{-2}$.

2. A semiconductor device according to claim 1 wherein the total amount of impurities of said third semiconductor layer between said second semiconductor layer and said fourth semiconductor layer is in the range of more than $10^{12}cm^{-2}$ and less than $10^{14}cm^{-2}$.

3. A semiconductor device according to claims 1 or 2, wherein the total amount of impurities of said third semiconductor layer between said second semiconductor layer and said fourth semiconductor layer is in the range or more than $10^{12}cm^{-2}$ and less than $10^{13}cm^{-2}$.

4. A semiconductor device according to any one of claims 1 to 3, wherein there is provided a concave selectively etched so as to reach said third semiconductor layer from the other main surface side through said fourth semiconductor layer.

5. A semiconductor device according to claim 4, wherein said control electrode is in ohmic-contact with the bottom of the concave.

6. A semiconductor device according to any one of the above claims, wherein the semiconductor substrate includes:

a fifth semiconductor of the first conductivity type, formed on the third semiconductor layer, of which impurity concentration is higher than that of the third semiconductor.

7. A semiconductor device according to claim 6, wherein said fifth semiconductor is formed on the third semiconductor layer between said second semiconductor layer and said fourth semiconductor layer.

8. A semiconductor device according to claims 6 or 7, as dependent on claim 4, and wherein said fifth semiconductor layer is formed on the bottom of the concave.

9. A semiconductor device according to claim 8, wherein said control electrode is in ohmic-contact with said fifth semiconductor layer formed on the bottom of the concave.

10. A semiconductor device according to any one of claims 6 to 9, wherein the total amount of the impurities of the third semiconductor layer is more than $1.2 \times 10^{11} cm^{-2}$, between said second semiconductor layer and a portion of said fifth semiconductor layer nearest to said second semiconductor layer.

11. A semiconductor device according to any one of claims 6 to 10, wherein the total amount of the impurities of the third semiconductor layer is more than $8 \times 10^{11} cm^{-2}$, between said fourth semiconductor layer and a portion of said fifth semiconductor layer nearest to said fourth semiconductor layer.

12. A semiconductor device according to claim 8 or 9, wherein the distance is in the range of more than 1 μm and less than 3 μm, from the bottom of said concave to a portion of said fifth semiconductor layer nearest to said second semiconductor layer.

13. A semiconductor device according to claim 6, wherein said fifth semiconductor layer is a buried layer formed in said third semiconductor layer, and the distance is in the range of more than 2 μm and less than 6 μm, between a portion of said fifth semiconductor layer nearest to said second semiconductor layer and one nearest to said second semiconductor layer.

14. A semiconductor device according to any one of the above claims, wherein a sixth semiconductor layer of the second conductivity type of which impurity concentration is higher than that of said second semiconductor layer, is provided on said second semiconductor layer, and wherein said sixth semiconductor layer is short-circuited on one main surface to said first semiconductor layer by said one main electrod .

15. A semiconductor device according to any one of the above claims, wherein a seventh semiconductor layer of the second conductivity type of which impurity concentration is higher than that of said second semiconductor layer, is provided between said first semiconductor layer and said second semiconductor layer.

16. A semiconductor device according to any one of the above claims, wherein an eighth semiconductor layer of the second conductivity type of which life time of carriers is higher than that of said second semiconductor layer, is provided between said first semiconductor layer and said second semiconductor layer.

17. A semiconductor device according to any one of the above claims, wherein the maximum value of the impurity concentration of said first semiconductor is less than $10^{18} cm^{-2}$.

18. A power converter comprising:

a pair of direct current terminals;

alternating current terminals of which the number is the same as the phase number of an alternating current; and

inverter units connected to an alternating terminal in which the interconnecting point of arms is different, the inverter unit having the two arms connected in serial and the arm being a parallel circuit of a switching element and a diode with inverse polarity and connected between the pair of direct current terminals;

wherein said switching element comprises;

a semiconductor device according to any one of the above claims.

FIG. 1A

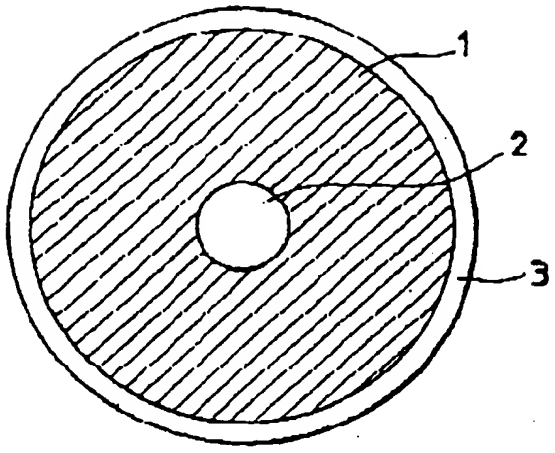


FIG. 1B

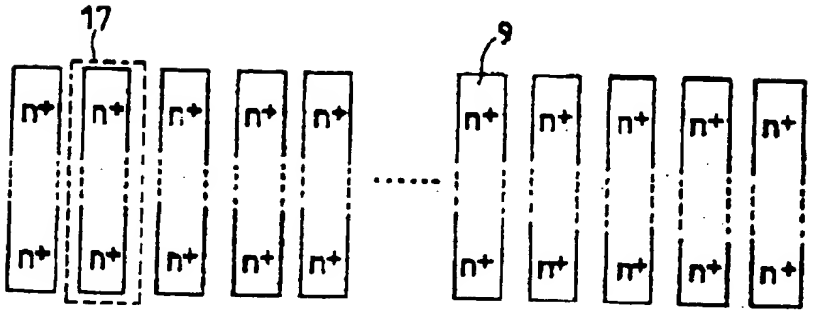


FIG. 1C

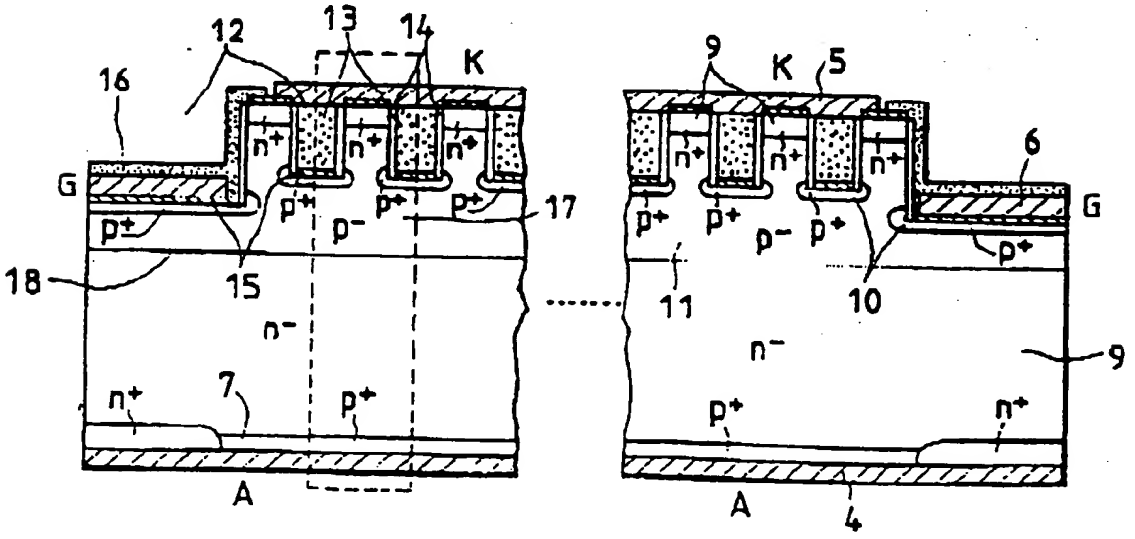


FIG. 2A

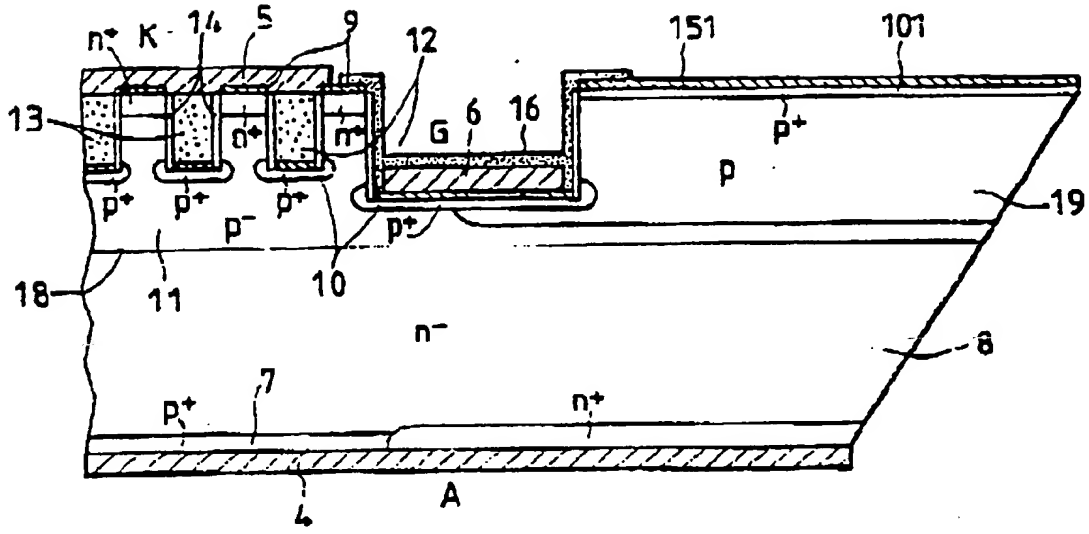

n+
K
14
5
9
12
151
101
13
n+
n+
G
6
16
p+
p
19
p+
p+
p+
p-
p+
18
11
10
n-
8
p+
7
n+
4
A

FIG. 2B

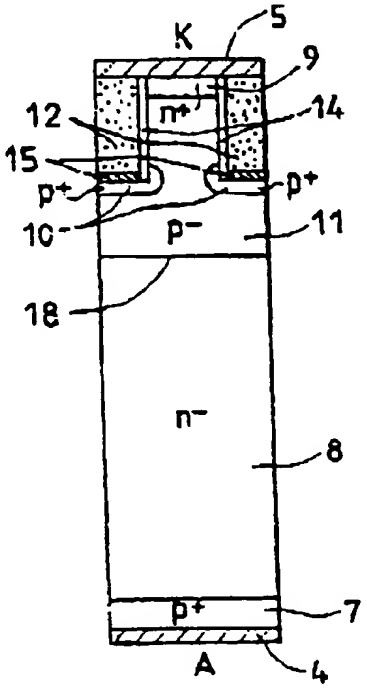

K
5
9
12
n+
14
15
p+
p+
10
p-
11
18
n-
8
p+
7
A
4

FIG. 3A

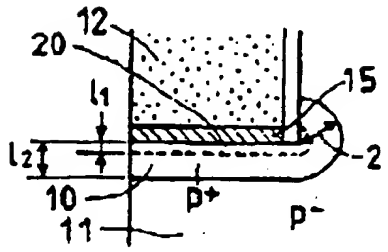


FIG. 3B

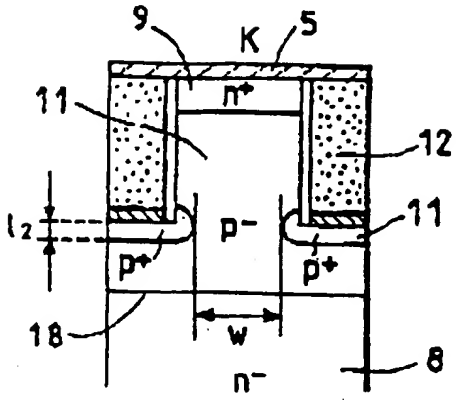


FIG. 3C

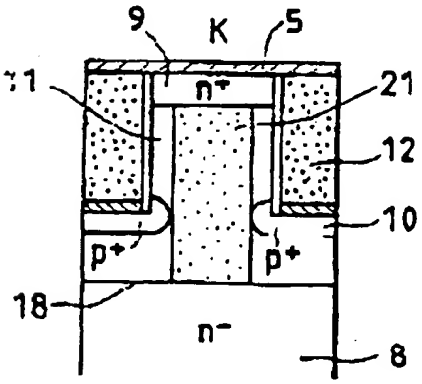


FIG. 3D

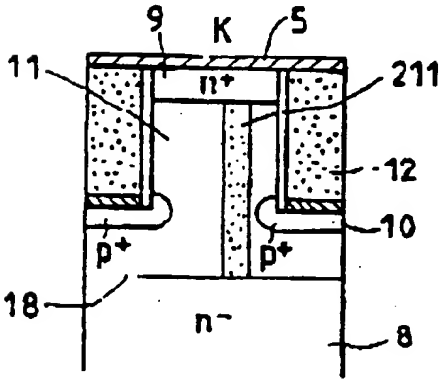


FIG. 3E

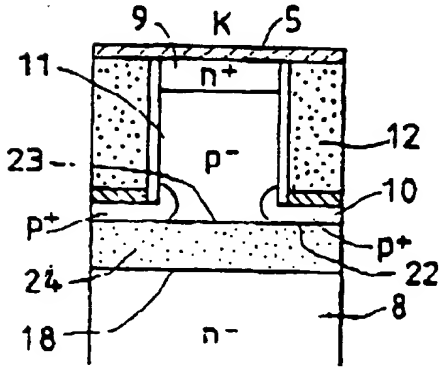


FIG. 3F

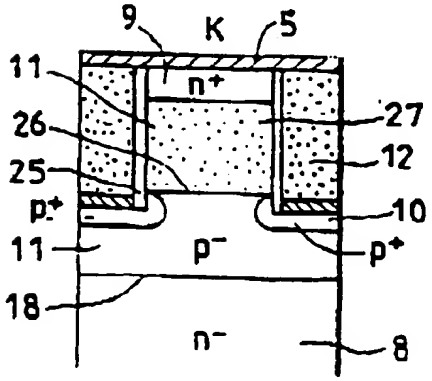


FIG. 4A

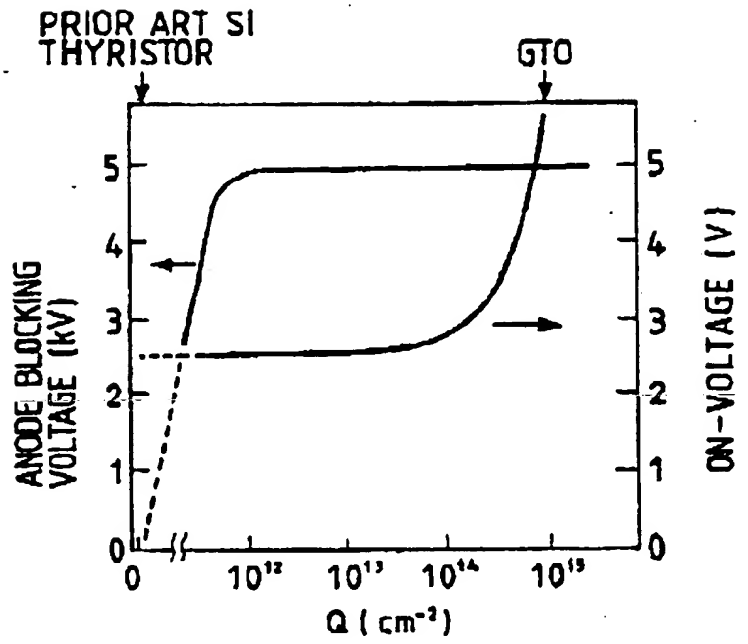

PRIOR ART SI THYRISTOR
GTO
ANODE BLOCKING VOLTAGE (kV)
ON-VOLTAGE (V)
0
1
2
3
4
5
10^{12}
10^{13}
10^{14}
10^{15}
Q (cm^{-2})

FIG. 4B

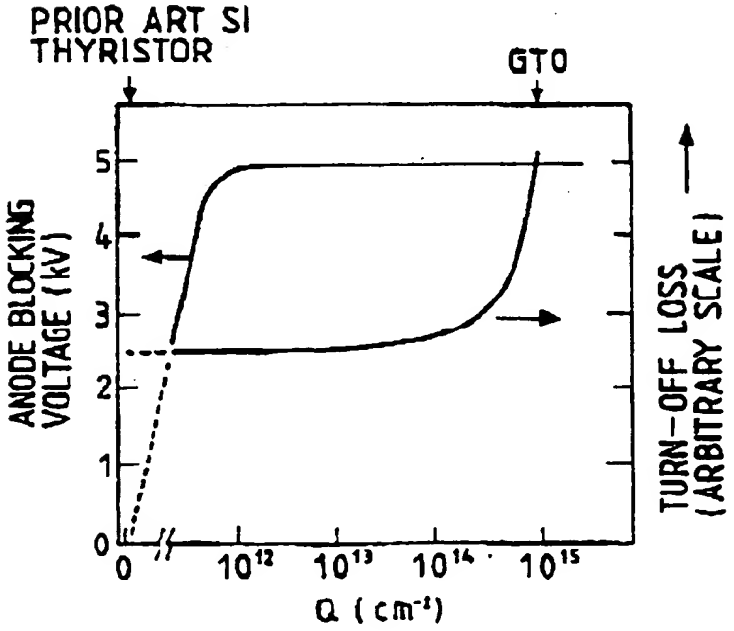

PRIOR ART SI THYRISTOR
GTO
ANODE BLOCKING VOLTAGE (kV)
TURN-OFF LOSS (ARBITRARY SCALE)
0
1
2
3
4
5
10^{12}
10^{13}
10^{14}
10^{15}
Q (cm^{-2})

FIG. 5

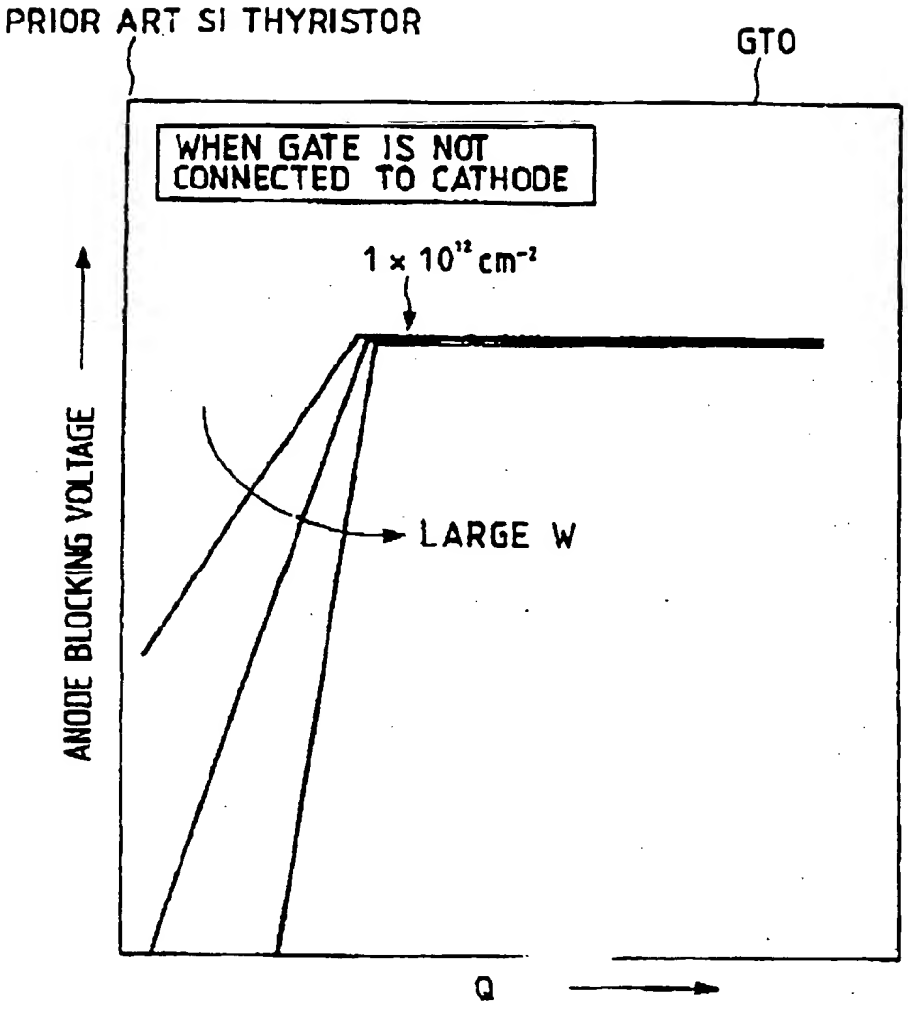
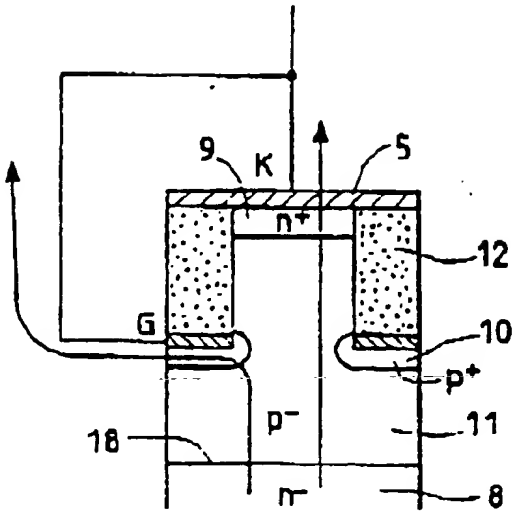
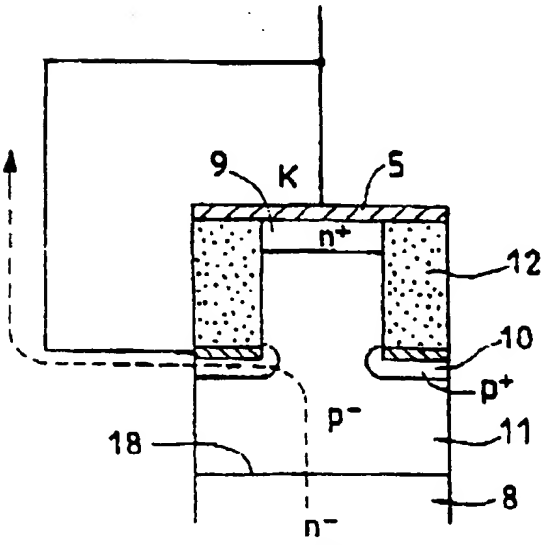

PRIOR ART SI THYRISTOR
GTO
WHEN GATE IS NOT CONNECTED TO CATHODE
1 × 10¹² cm⁻²
LARGE W
ANODE BLOCKING VOLTAGE
Q

FIG. 6A



$Q < 10^{12}\ cm^{-2}$

FIG. 6B



$Q \geq 10^{12}\ cm^{-2}$

FIG. 7

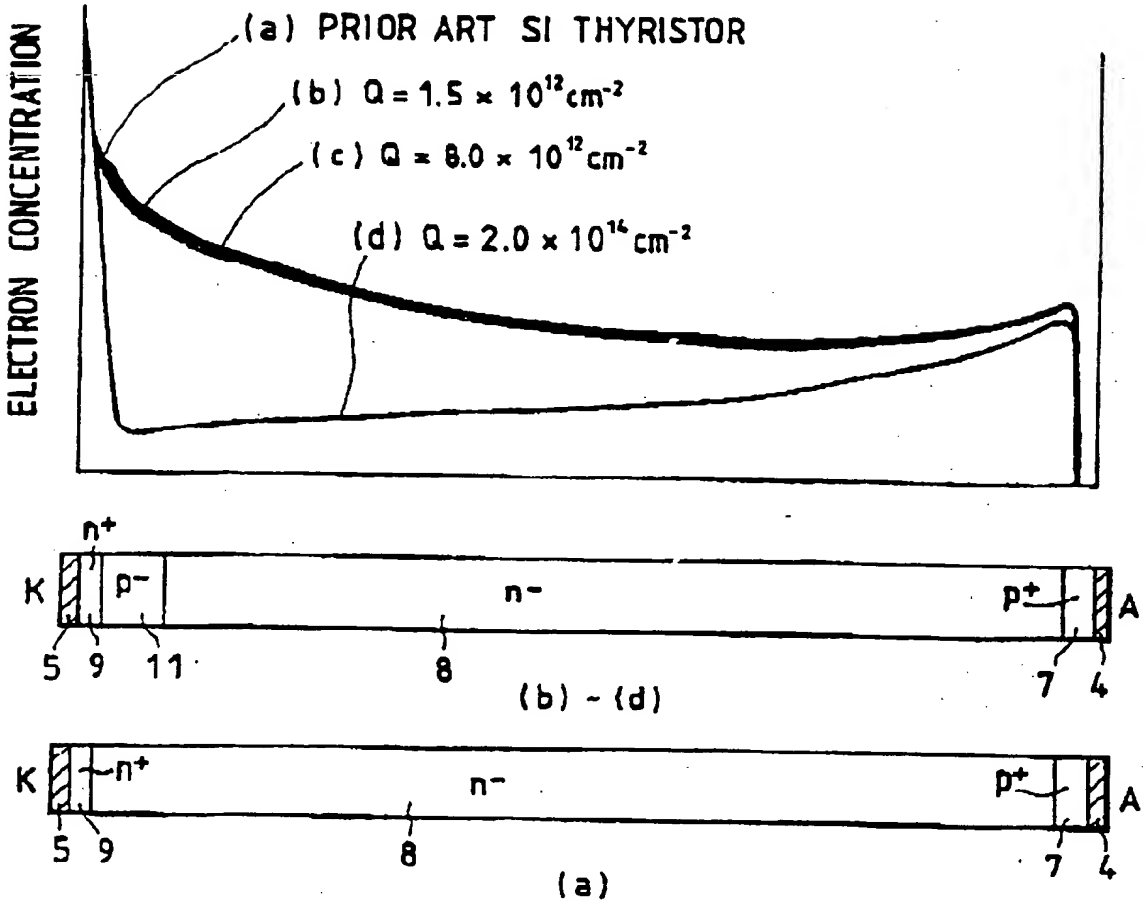

ELECTRON CONCENTRATION
(a) PRIOR ART SI THYRISTOR
(b) Q = 1.5 × 10^12 cm^-2
(c) Q = 8.0 × 10^12 cm^-2
(d) Q = 2.0 × 10^14 cm^-2
n+
K
p-
n-
p+
A
5
9
11
8
7
4
(b) ~ (d)
K
n+
n-
p+
A
5
9
8
7
4
(a)

FIG. 8

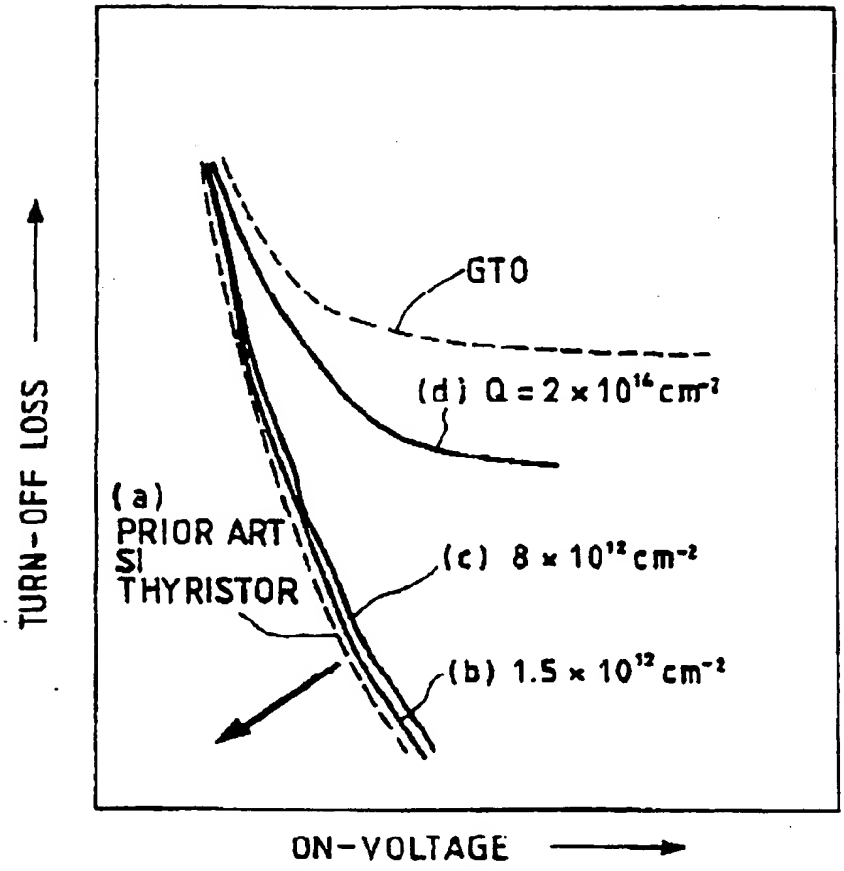

GTO
(d) Q = 2 × 10¹⁶ cm⁻²
(a)
PRIOR ART
SI
THYRISTOR
(c) 8 × 10¹² cm⁻²
(b) 1.5 × 10¹² cm⁻²
TURN-OFF LOSS
ON-VOLTAGE

FIG. 9A

FIG. 9B

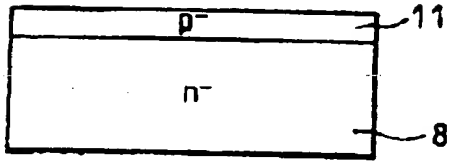


FIG. 9C

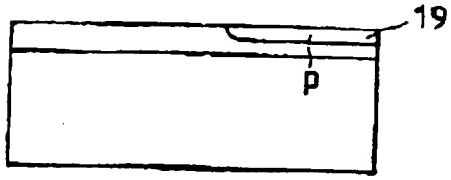


FIG. 9D

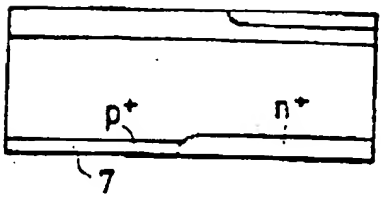


FIG. 9E

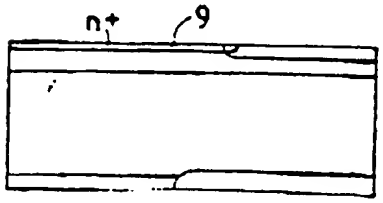


FIG. 9F

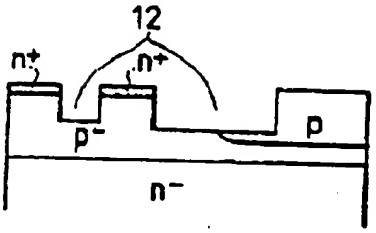


FIG. 9G

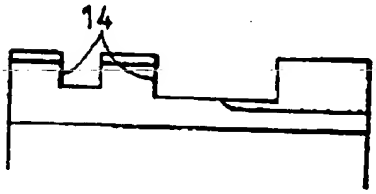


FIG. 9H

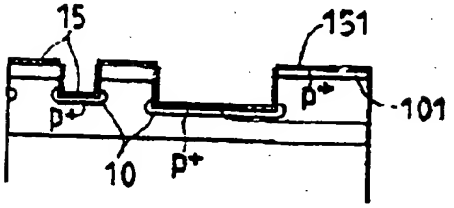


FIG. 9I

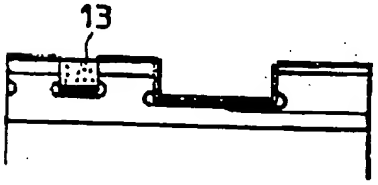


FIG. 9J

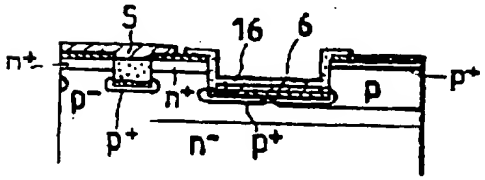


FIG. 10A

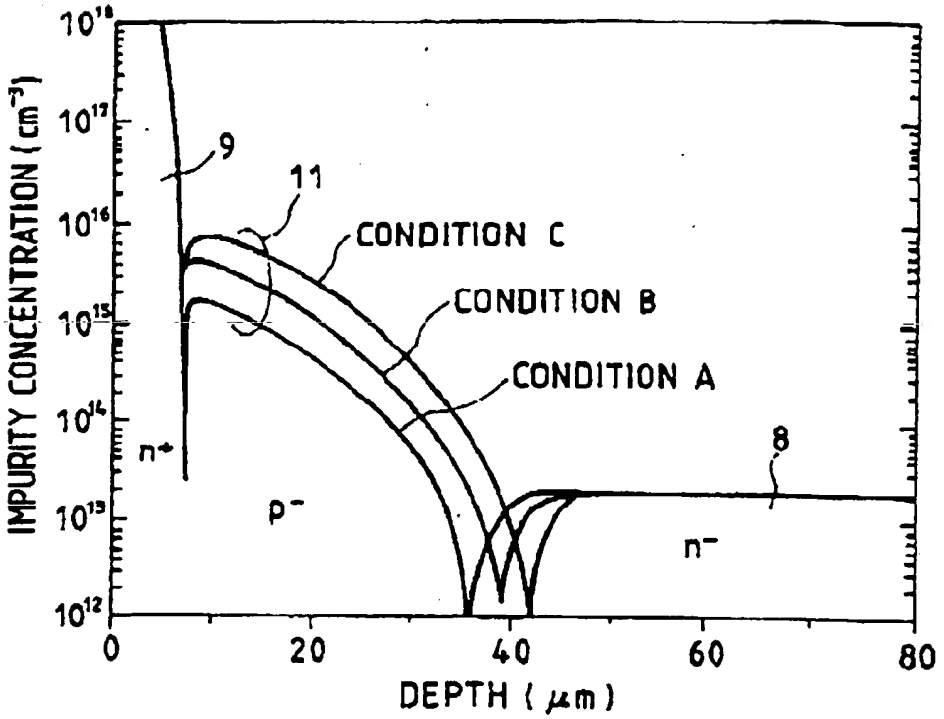
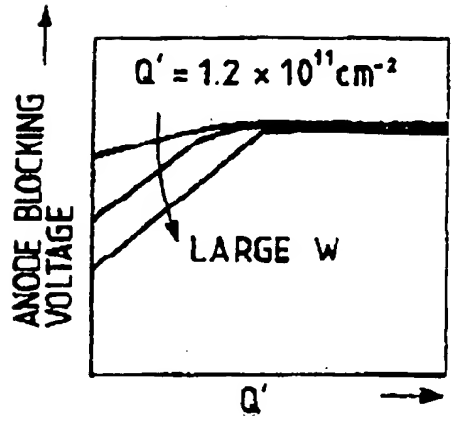


FIG. 10B

	THICKNESS (μm)	MAXIMUM IMPURITY CONCENTRATION ($\times 10^{15}cm^{-3}$)	Q ($\times 10^{12}cm^{-2}$)	Q' ($\times 10^{11}cm^{-2}$)	Q'' ($\times 10^{12}cm^{-2}$)
CONDITION A	28	1.5	1.5	2	1
CONDITION B	30	4	4	5	3
CONDITION C	33	7	8	12	7

DEPTH OF GROOVE : 20μm 12 : 2μm
MAXIMUM IMPURITY CONCENTRATION IN GATE p^+ LAYER : $5 \times 10^{19}cm^{-3}$

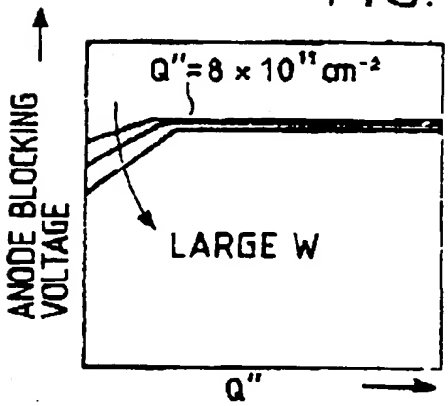
FIG. 11A



$Q \geq 10^{12}\ cm^{-2}$
$Q'' \geq 8 \times 10^{11} cm^{-2}$

VOLTAGE ACROSS GATE AND CATHODE : 0V

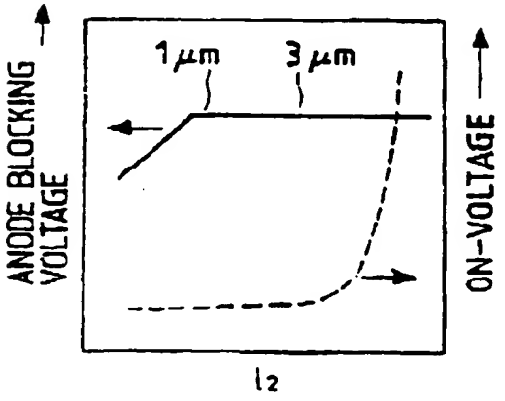
FIG. 11B



$Q \geq 10^{12}\ cm^{-2}$
$Q' \geq 1.2 \times 10^{11} cm^{-2}$

VOLTAGE ACROSS GATE AND CATHODE : -100V

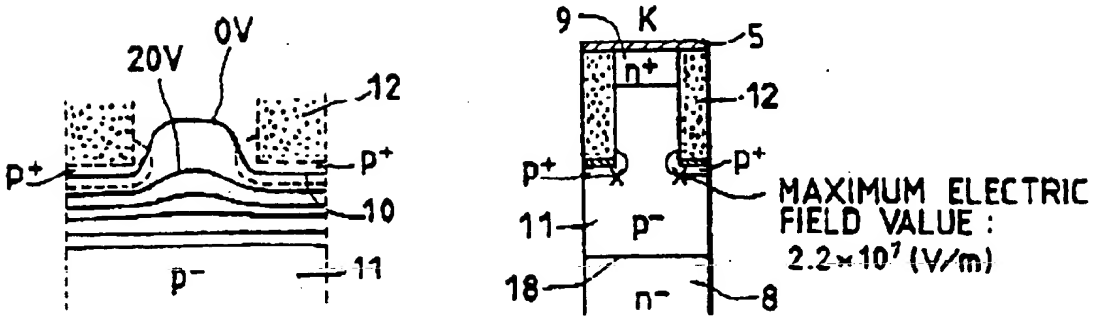
FIG. 11C



$Q \geq 10^{12}\ cm^{-2}$
$Q' \geq 1.2 \times 10^{11} cm^{-2}$
$Q'' \geq 8 \times 10^{11} cm^{-2}$

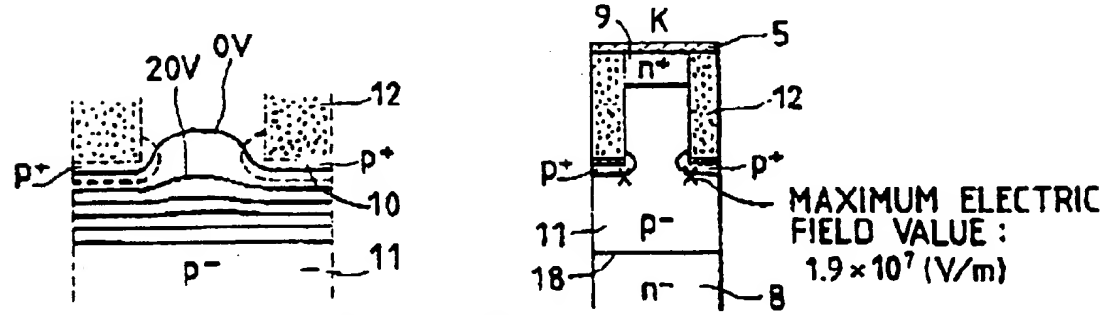
FIG. 12A

X----POSITION WHERE ELECTRIC FIELD IS MAXIMUM
EQUIPOTENTIAL LINE : 20V/div
$Q' > 10^{12}cm$, $Q'' > 8 \times 10^{11}cm$



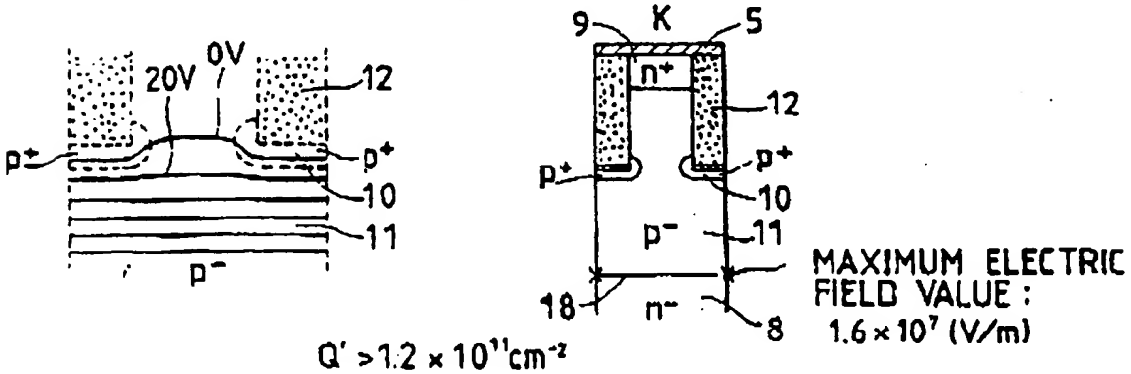
$Q' < 1.2 \times 10^{11} cm^{-2}$

FIG. 12B



$Q' > 1.2 \times 10^{11} cm^{-2}$

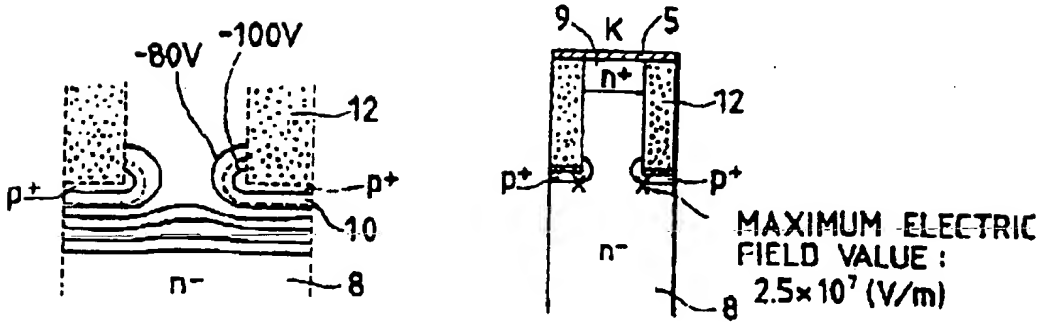
FIG. 12C



$Q' > 1.2 \times 10^{11} cm^{-2}$

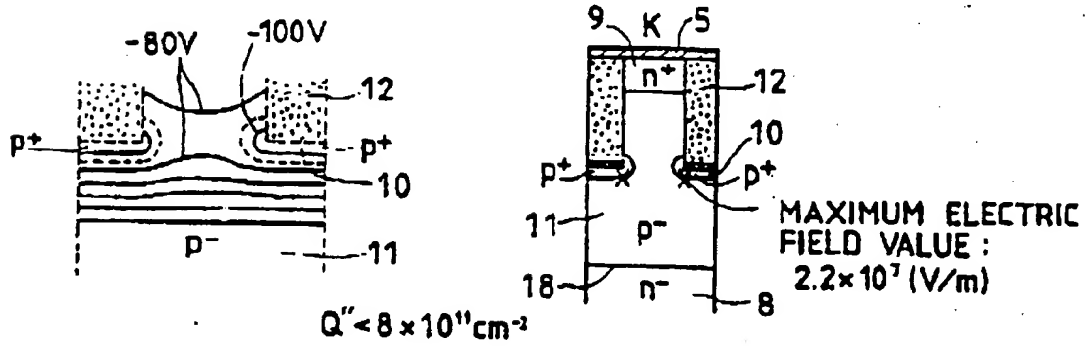
FIG. 13A

X---POSITION WHERE ELECTRIC FIELD IS MAXIMUM
EQUIPOTENTIAL LINE : 20V/div
$Q > 10^{12}$cm, $Q' > 1.2 \times 10^{11}$cm



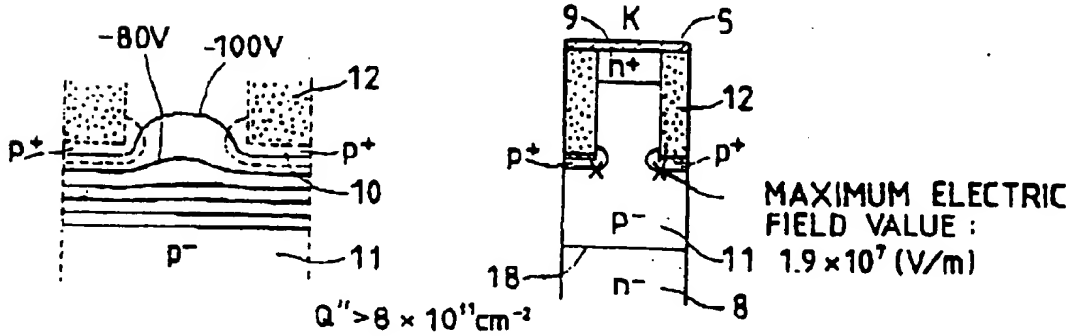
CONVENTIONAL SI THYRISTOR

FIG. 13B



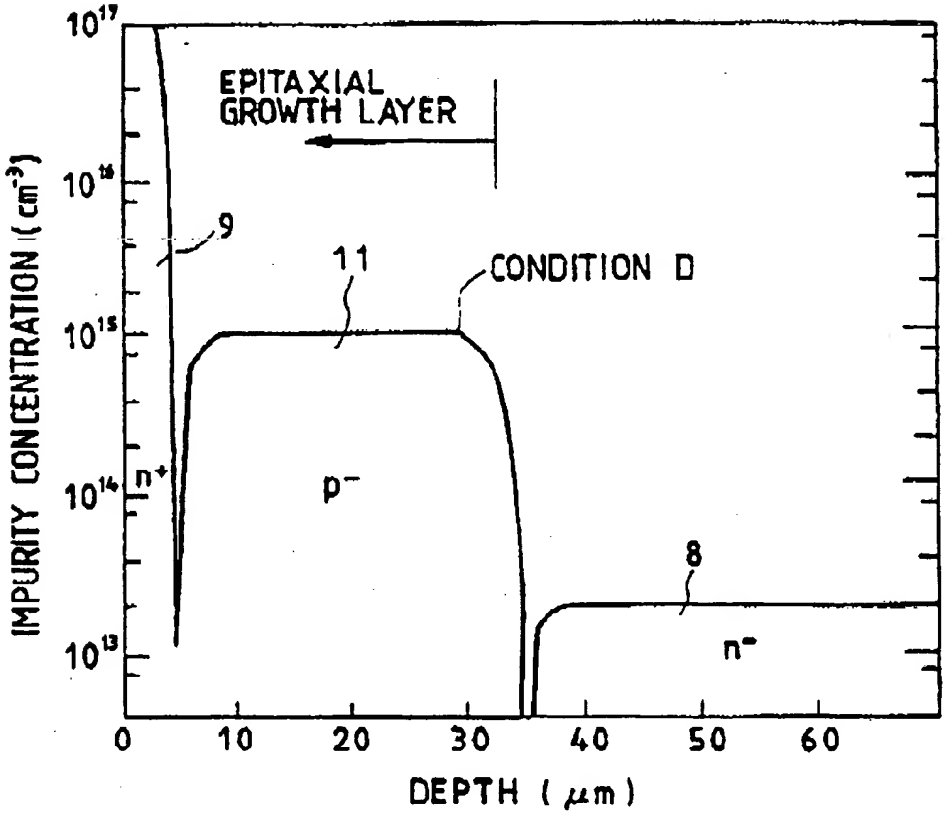
$Q'' < 8 \times 10^{11}cm^{-2}$

FIG. 13C



$Q'' > 8 \times 10^{11}cm^{-2}$

FIG. 14



CONDITION D	THICKNESS (μm)	: 29
	MAXIMUM IMPURITY CONCENTRATION ($\times 10^{15}cm^{-3}$)	: 1
	Q ($\times 10^{12}cm^{-2}$)	: 3
	Q' ($\times 10^{11}cm^{-2}$)	: 13
	Q'' ($\times 10^{12}cm^{-2}$)	: 1.2
	DEPTH OF GROOVE	: 20 μm, l_2 : 2 μm
	MAXIMUM IMPURITY CONCENTRATION IN GATE p^+ LAYER	: $5 \times 10^{19}cm^{-3}$

FIG. 15A

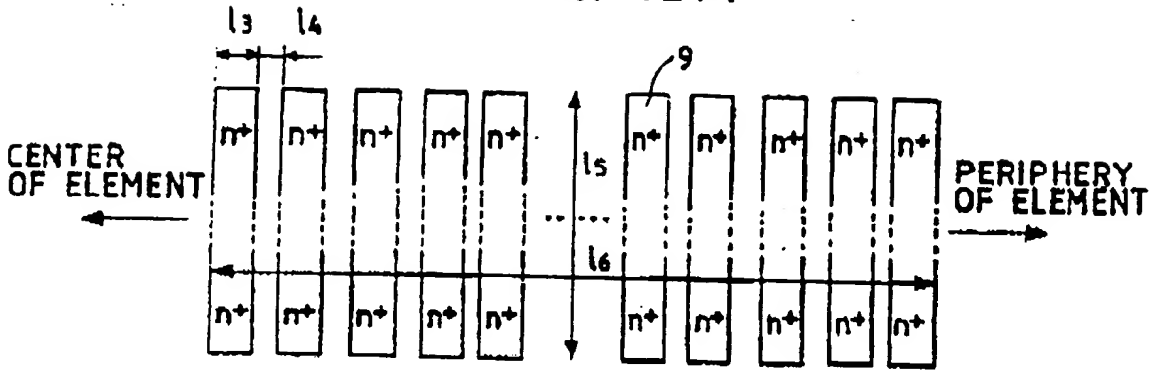


FIG. 15B

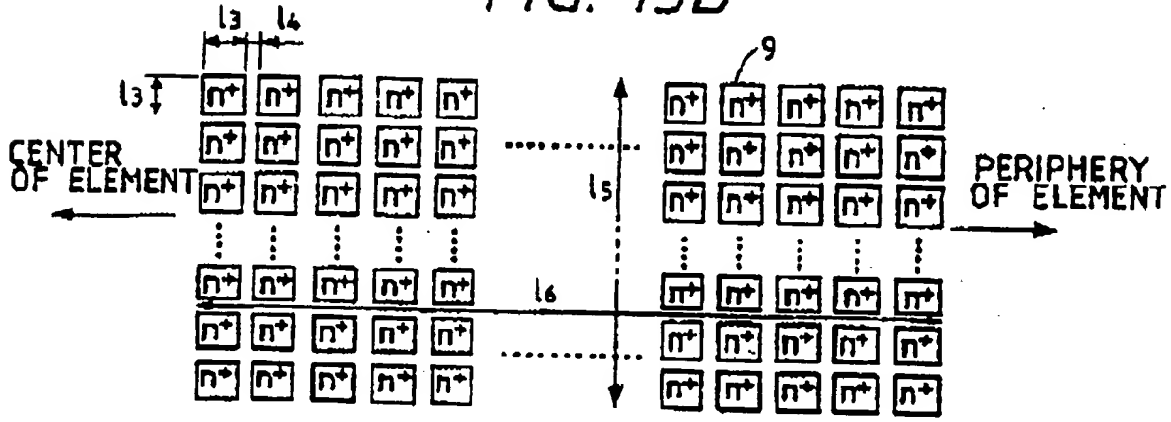


FIG. 15C

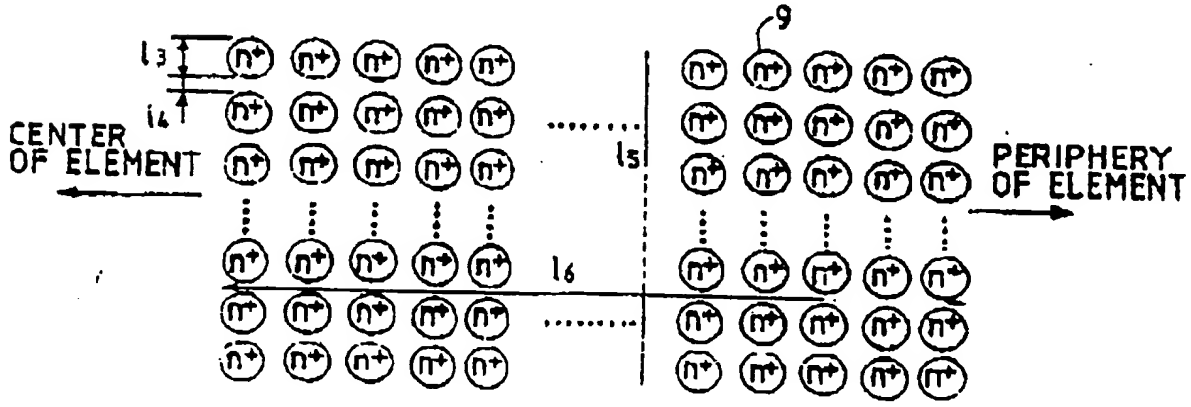


FIG. 16A

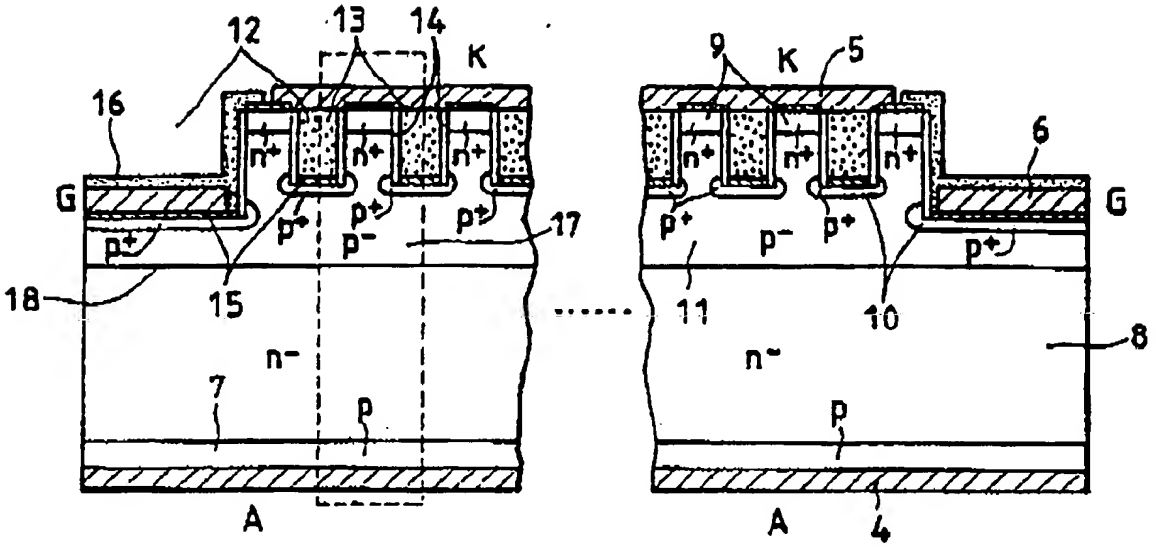


FIG. 16B

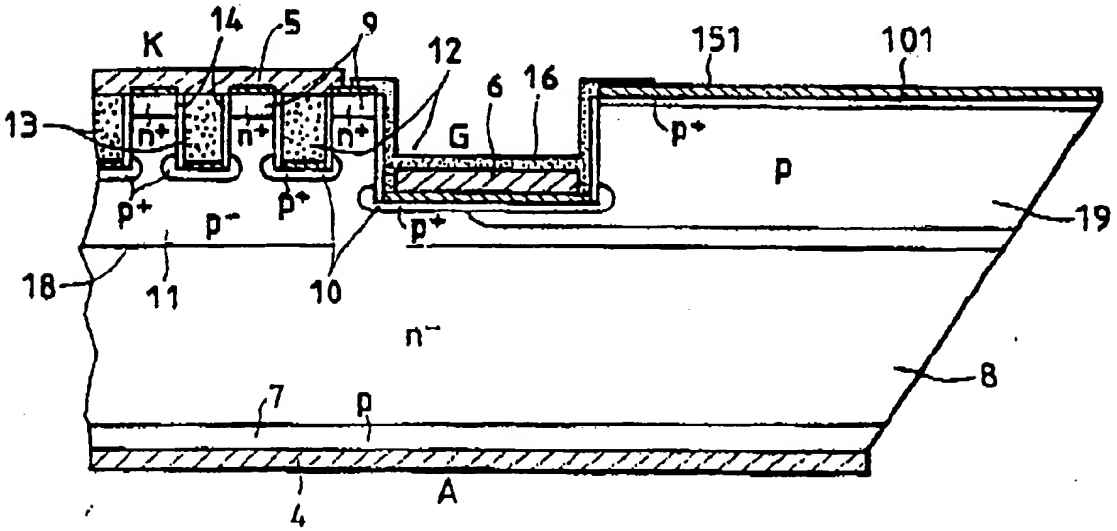


FIG. 17A

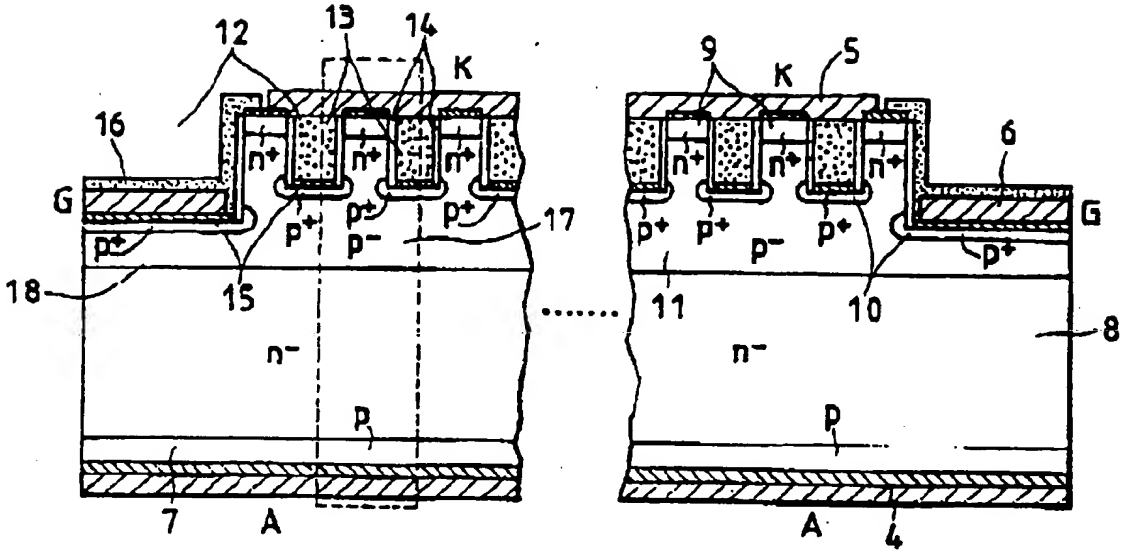


FIG. 17B

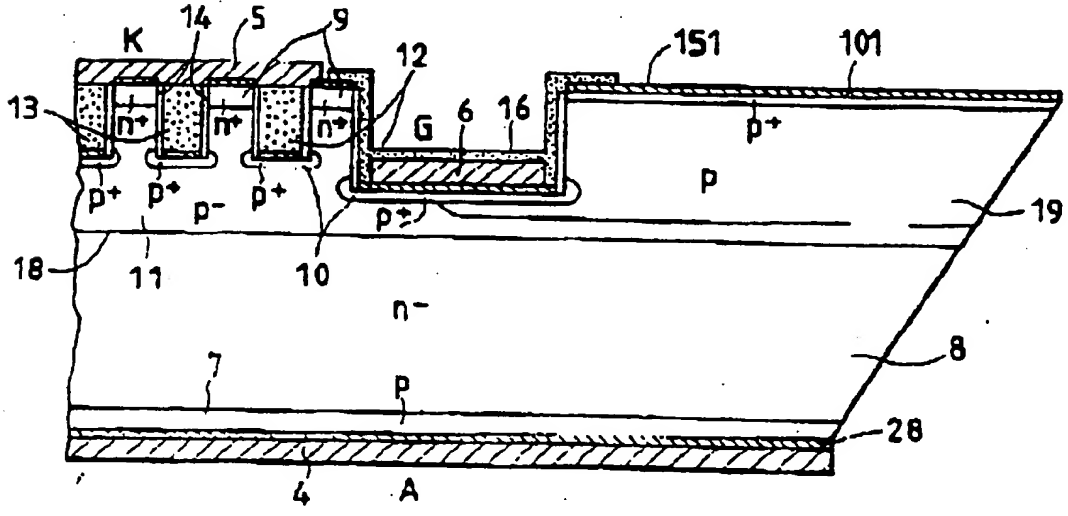


FIG. 18A

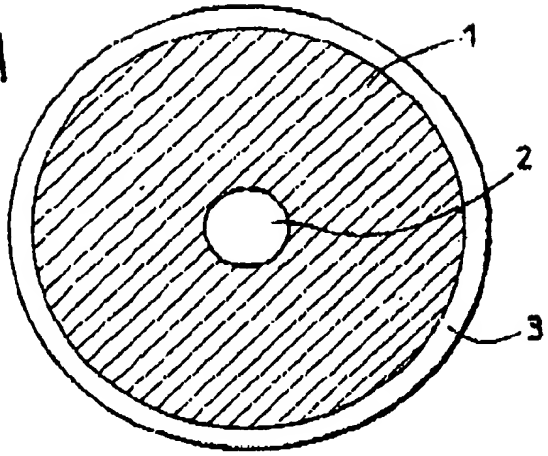


FIG. 18B

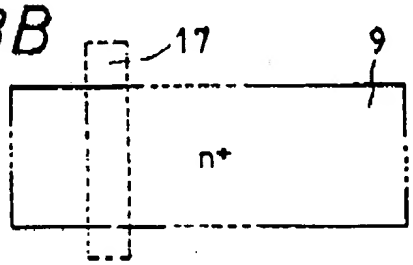


FIG. 18C

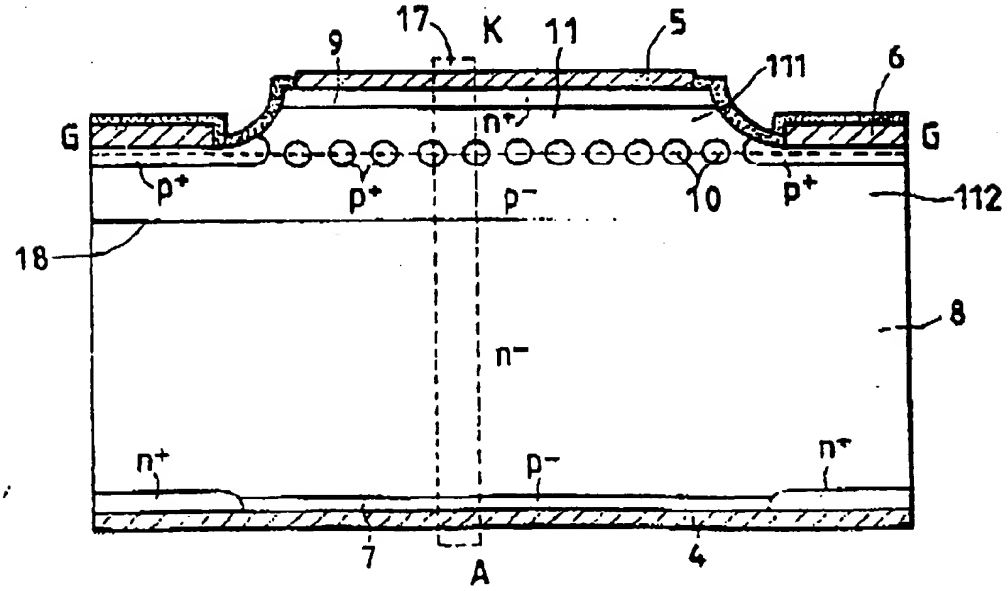


FIG. 19A

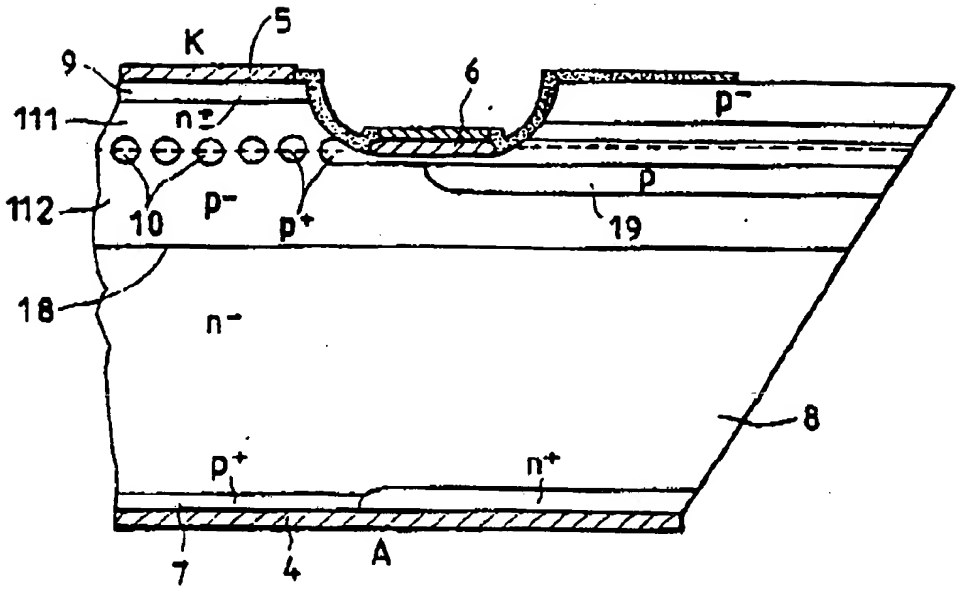


FIG. 19B

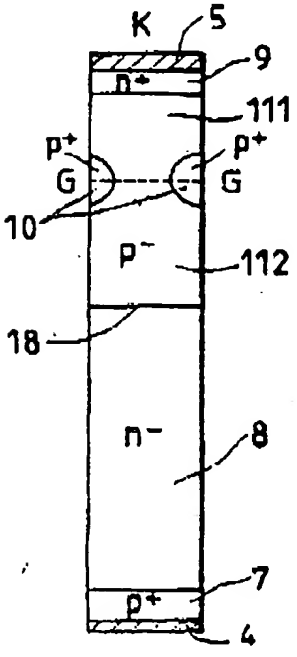


FIG. 19C

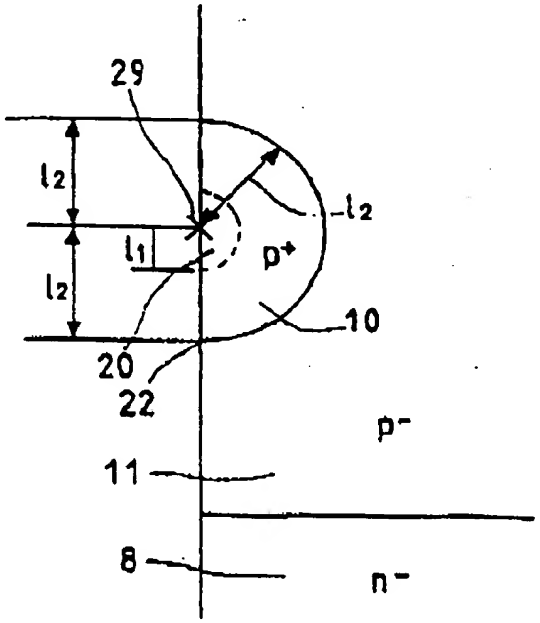


FIG. 20A

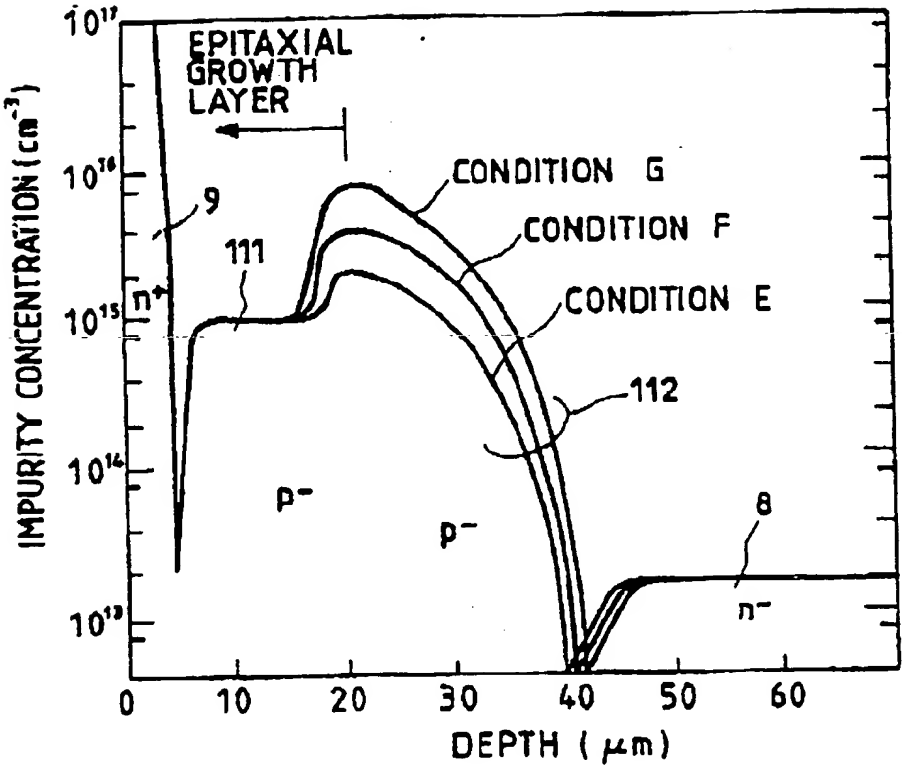


FIG. 20B

	THICKNESS (μm)	MAXIMUM IMPURITY CONCENTRATION (×10¹⁵ cm⁻³)	Q (×10¹² cm⁻²)	Q' (×10¹¹ cm⁻²)	Q'' (×10¹² cm⁻²)
CONDITION E	35	2	4	9	1.7
CONDITION F	36	4	6.5	20	1.7
CONDITION G	37	8	10	36	1.7

FIG. 21A

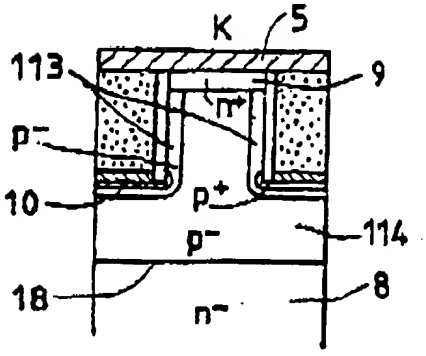


FIG. 21B

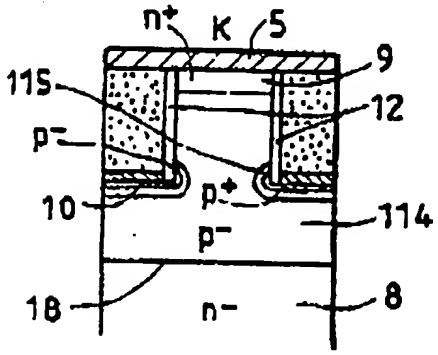


FIG. 21C

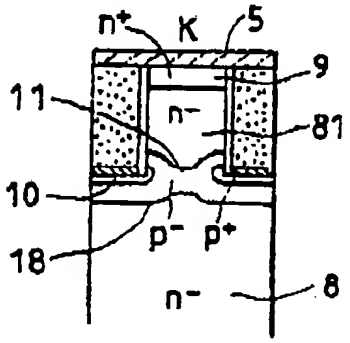


FIG. 21D

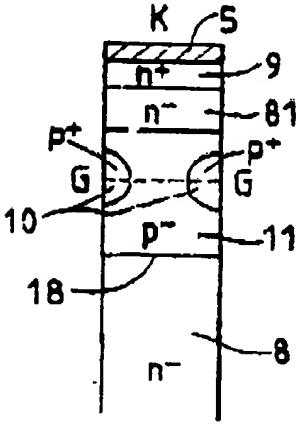


FIG. 21E

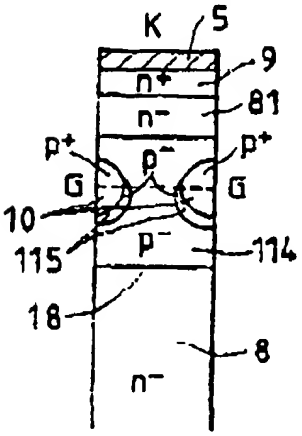


FIG. 21F

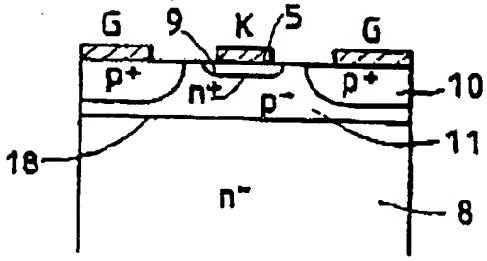


FIG. 22

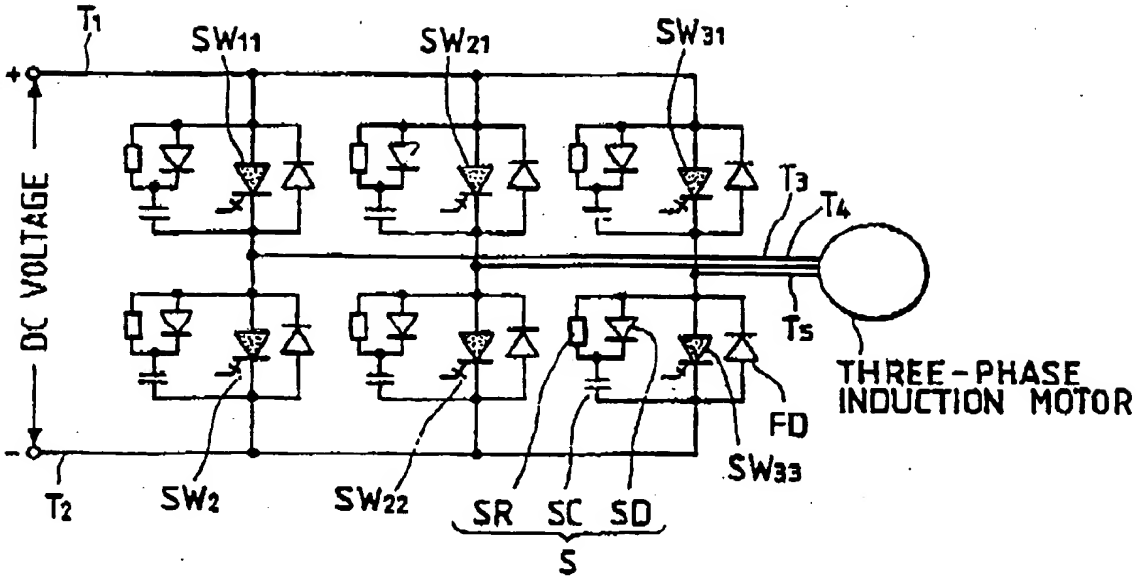

T1
SW11
SW21
SW31
+
DC VOLTAGE
-
T3
T4
Ts
THREE-PHASE
INDUCTION MOTOR
FD
SW33
T2
SW2
SW22
SR SC SD
S

FIG. 23A

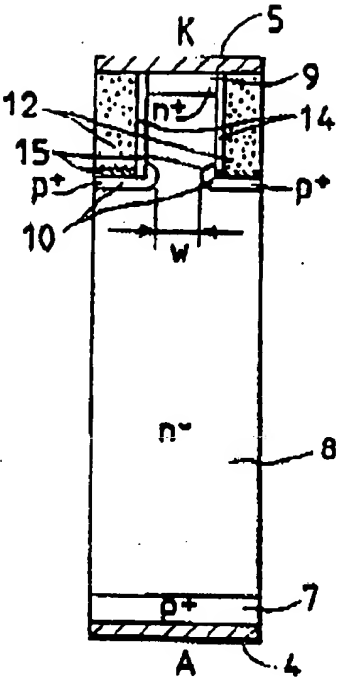
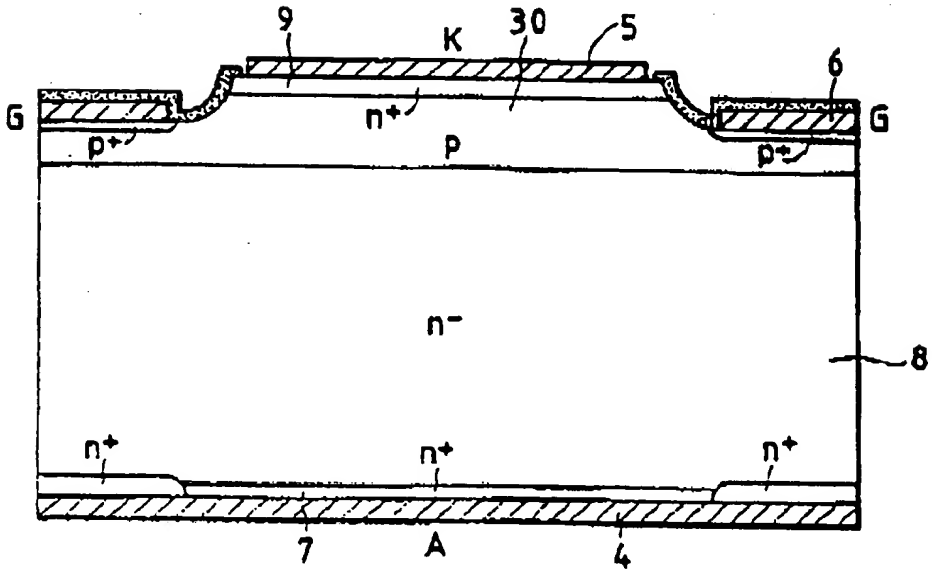


FIG. 23B



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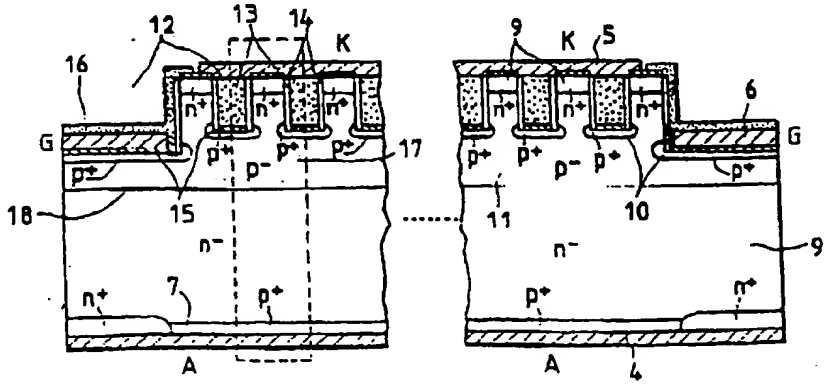
(54) Semiconductor switching device and power converter

(57) There is provided a semiconductor substrate which includes a pair of main surfaces, a first semiconductor layer (7) of a first conductivity type adjacent to one of the main surface, a second semiconductor layer (8) of a second conducting type of which impurity concentration is lower than that of the first semiconductor layer and which is adjacent to the first semiconductivity, a third semiconductor layer (11) of the first conductivity type adjacent to the second semiconductor, and a fourth semiconductor (9) of the second conductivity type of which impurity concentration is higher than that of the third semiconductor and which is adjacent to the other of the main surfaces and the third semiconductor. The device further includes one main electrode (4) in ohmic-contact with the first semiconductor layer on one of the main surfaces of said semiconductor substrate, the other main electrode (5) in ohmic-contact with the first semiconductor layer on the other of the main surfaces of said semiconductor substrate, and a control electrode (6) connected electrically to the third semiconductor layer. The total amount of impurities of said third semiconductor layer is less than $10^{14}cm^{-2}$.

FIG. 1C



EP 0 696 066 A3

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Application Number
EP 95 30 4623

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 239 866 A (BBC AG BROWN, BOVERI & CIE) * column 7, line 27 - line 28; figure 5 *	1-18	H01L29/744 H01L29/739
X	EP 0 178 387 A (BBC BROWN BOVERI AG) * page 9, line 31 - page 10, line 11; figure 4 *	1-18	
X	EP 0 121 068 A (BBC AG BROWN, BOVERI & CIE) * page 8, line 9 - line 11; figures * * page 11, line 13 - line 14 *	1-18	
A	US 4 198 645 A (SEMICONDUCTOR RESEARCH FOUNDATION) * abstract; figures 1,2 *	1-18	
A	US 4 752 818 A (KABUSHIKI KAISHA TOSHIBA CHUO KENKYUSHO) * abstract; figures *	16	
A	PATENT ABSTRACTS OF JAPAN vol. 8, no. 161 (E-257), 26 July 1984 & JP 59 059070 A (HITACHI SEISAKUSHO KK), 4 April 1984, * abstract *	18	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 April 1998	Sinemus, M

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